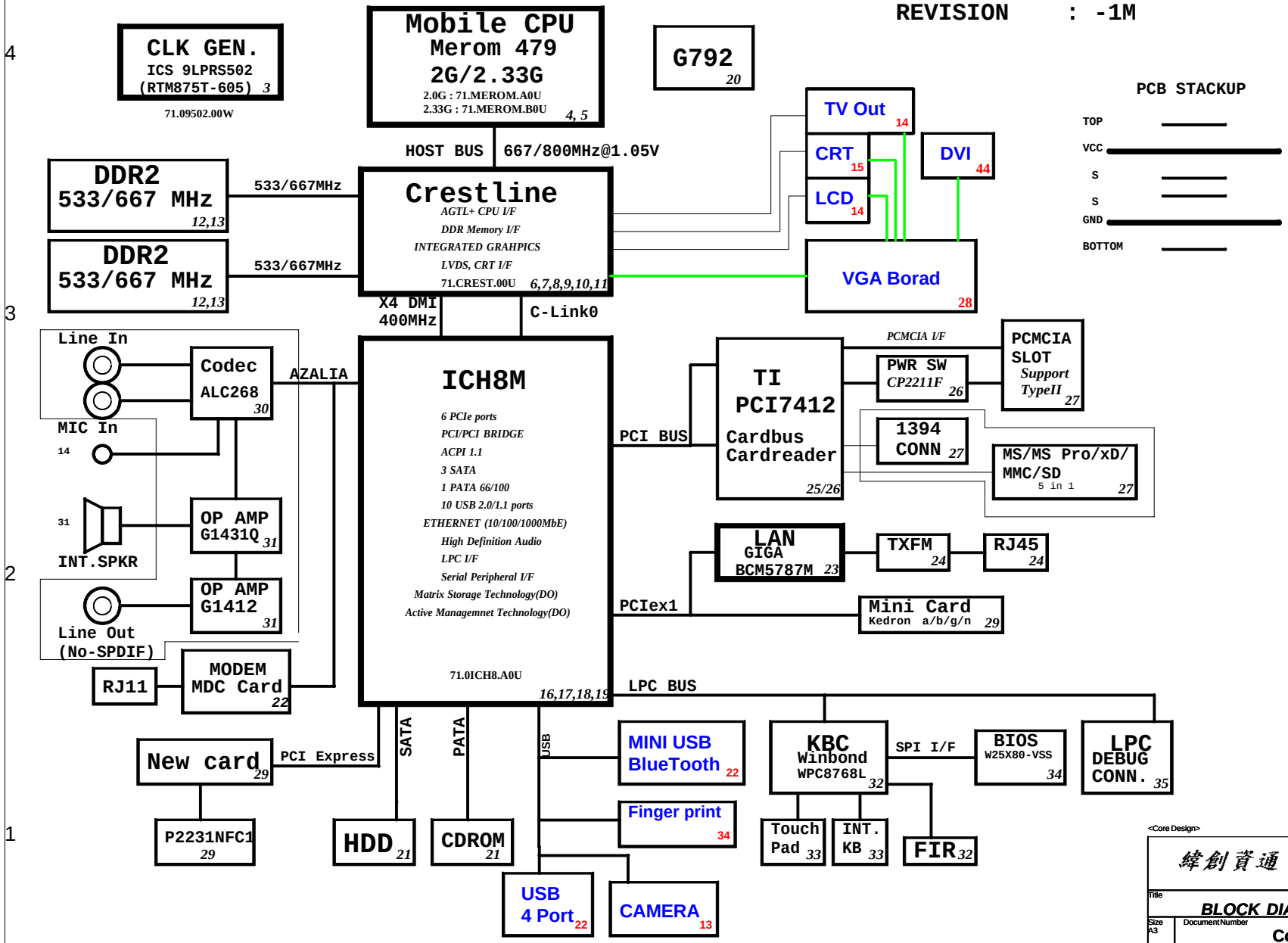
Columbia/Tangiz Block Diagram

Project code: 91.4T301.001
PCB P/N : 48.4T301.01M
REVISION : -1M



SYSTEM DC/DC MAX8744 38	
INPUTS	OUTPUTS
DCBATOUT	5V_S5(6A) 3D3V_S5(7A)

SYSTEM DC/DC Max8717 39	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0(9.5A) 1D8V_S3(8.5A)
TPS51100 41	
1D8V_S3	DDR_VREF_S0 (1.5A) DDR_VREF_S3
APL5915 41	
1D8V_S3	1D25V_S0 (2A)
APL531230	
3D3V_S0	2D5V_S0 (300mA)
APW5912 40	
3D3V_S5	1D5V_S3 (7.5A)

ISL CHARGER ISL6255 41	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 4.0A UP+5V 5V 100mA

CPU DC/DC MAX8770 35,36	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.3V 47A

<Core Design>

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Title: BLOCK DIAGRAM

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ICH8M Functional Strap Definitions

ICH8-M EDS 21762 2.0V1 page 16

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h)
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE config2 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#/ SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05, VccSus1_5 and VccCL1_5 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05, VccSus1_5 and VccCL1_5 VRM's when sampled high
LAN100_SLP	Integrated VccLAN1_05 and VccCL1_05 VRM Enable/Disable. Always sampled.	Enables integrated VccLAN1_05 and VccCL1_05 VRM's when sampled high
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	This signal has a weak internal pull-up. Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be used in manufacturing environments.

ICH8M Integrated Pull-up and Pull-down Resistors

ICH8-M EDS 21762 2.0V1

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 10K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	PULL-UP 13K

Crestline Strapping Signals and Configuration

Crestline EDS 20954 1.0 page 7

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG[8:6]	Reserved	
	Low Power PCI Express	0 = Normal mode **1 = Low Power mode** (Default)
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled **11 = Normal Operation** (Default)
CFG[15:14]	Reserved	Reserved
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	**0 = Normal operation (Default):lane Numbered in order** 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	**0 = Only SDVO or PCIE x1 is operational (Default)** 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCRTL _DATA	SDVO Present	**0 = No SDVO Card present** (Default) 1= SDVO Card present

NOTE: All strap signals are sampled with respect to the leading edge of the Crestline GMCH PWORK in signal.

History

ICH8M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm

PCI Routing

page 17

	IDSEL	INT	REQ	GNT
TI7412	AD22	G:CARDBUS B:1394 F:Flash Media G:SD Host	0	0

PCIE Routing

LANE1	LAN BCM5787M
LANE2	MiniCard WLAN
LANE3	NewCard WLAN

USB Table

USB	
Pair	Device
0	USB1
1	NC
2	USB2
3	USB4
4	USB3
5	BLUETOOTH
6	WEBCAM
7	FT
8	MINICARD
9	NEW1

UMA

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Title: Reference

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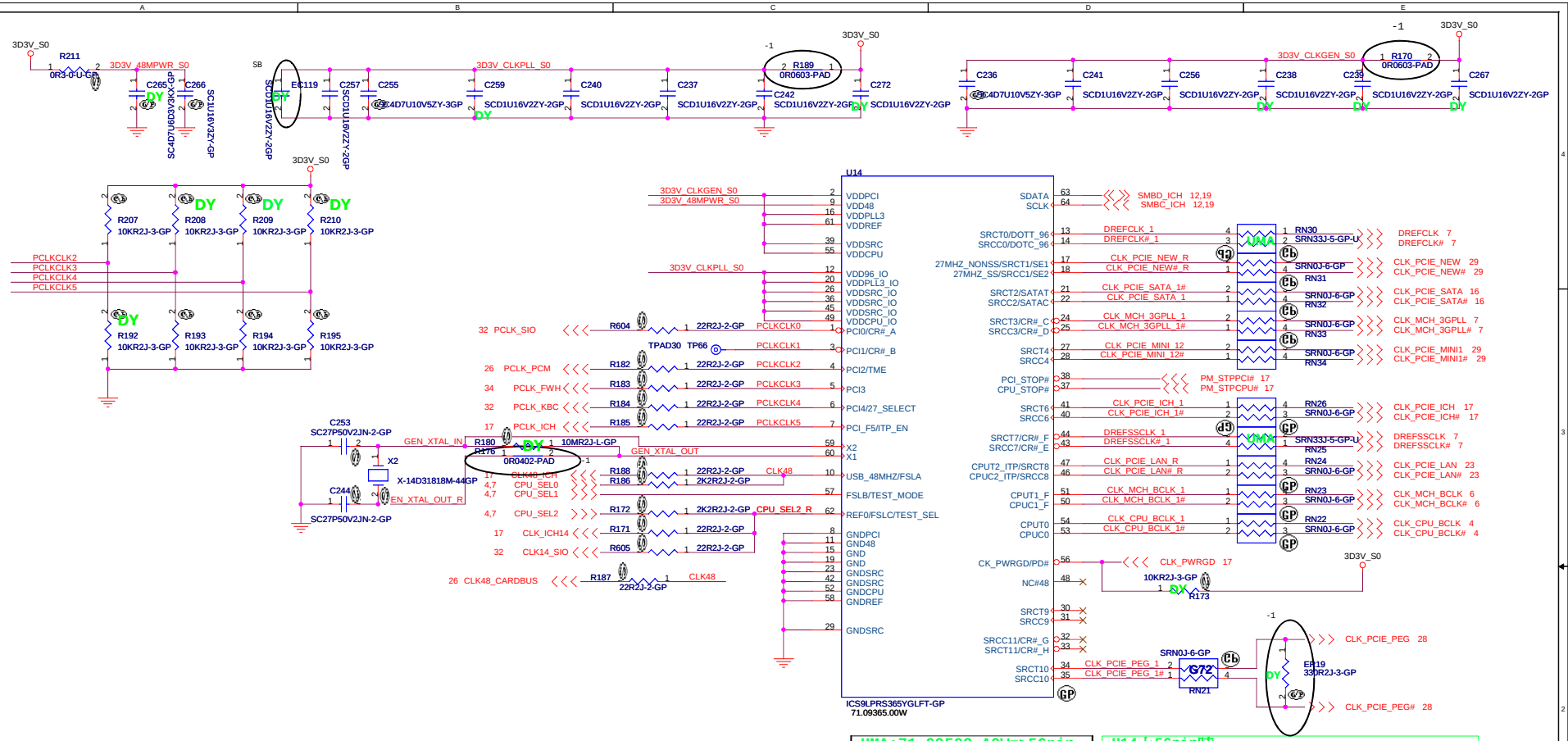

UMA:71.09502.A0W=>56pin
G72:71.09365.00W=>64pin

U14上56pin時
RN22,23,24,26,31,32,33,34改成66.33036.04L

ICS9LPR502HGLFT-GP setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI4/SRC5_EN	0 = Pin29 as CPU_STOP# , pin 30 as PCI_STOP#. 1 = Pins29,30 as SRC-5 differential pair.
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#

RTM875T-605 setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3/SRC-5_EN	0 = Pin20 as CPU_STOP# , pin 30 as PCI_STOP#. 1 = Pins20,30 as SRC-5 differential pair.
PCI4/27M_SEL	0 = Pin17 as SRC-1, Pin18 as SRC-1#, Pin13 as DOT96, Pin14 as DOT96# 1 = Pin17 as 27MHz, Pin 18 as 27MHz_SS, Pin13 as SRC-0, Pin14 as SRC-0#
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	X
0	1	1	166M	667M
0	1	0	200M	800M

UMA

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Title: Clock Generator

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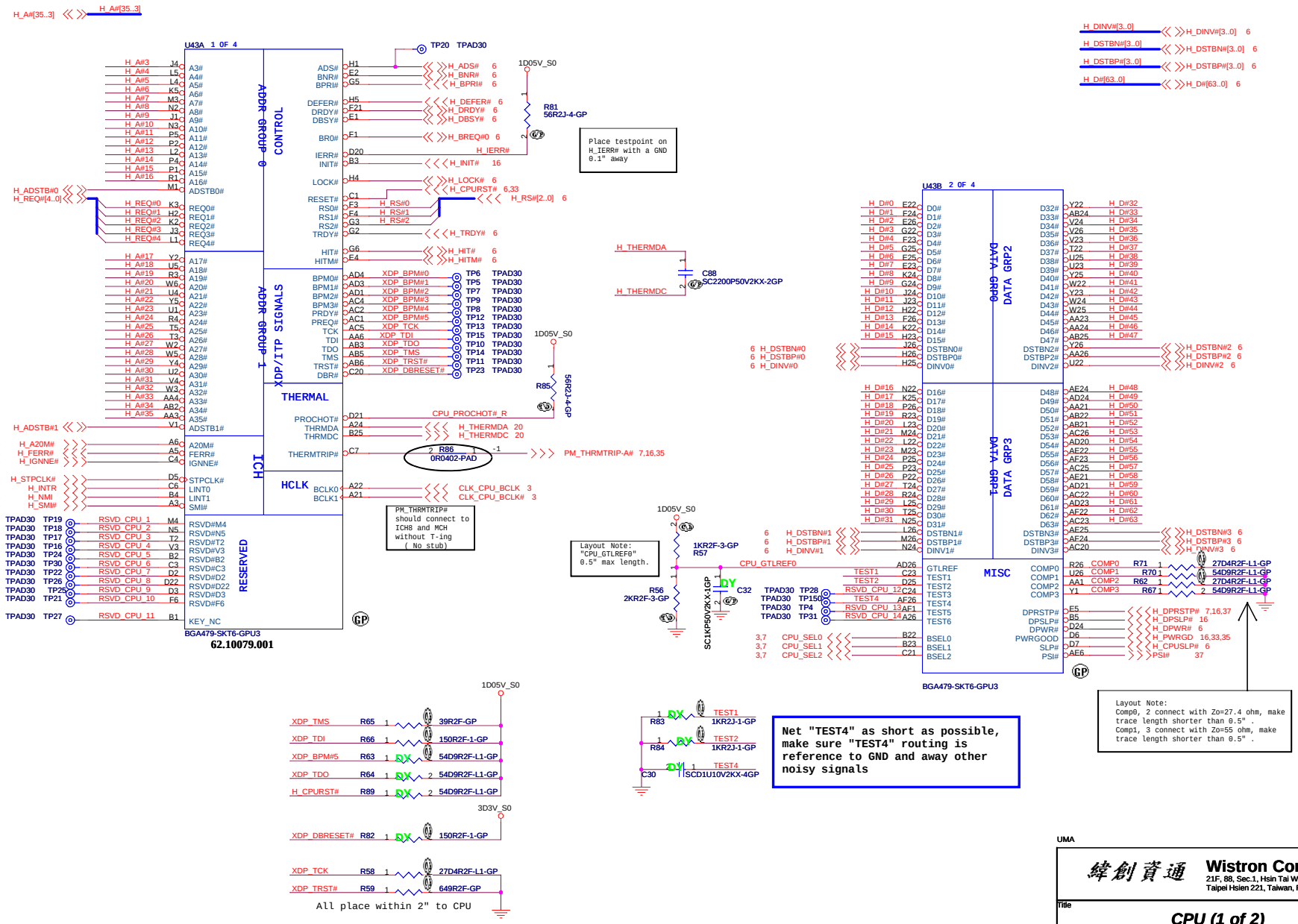

UMA

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Title: CPU (1 of 2)

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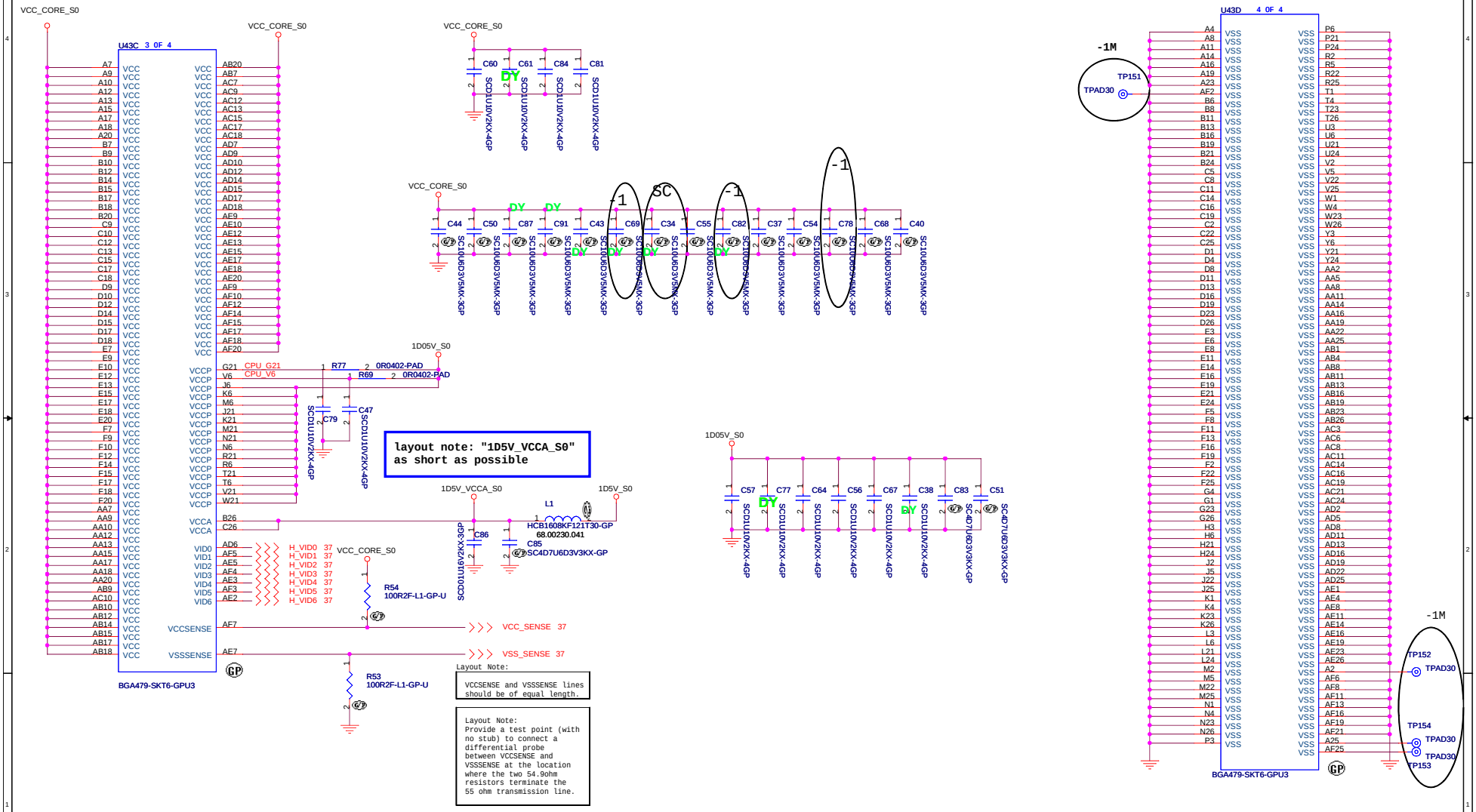

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Title	***CPU (2 of 2)***
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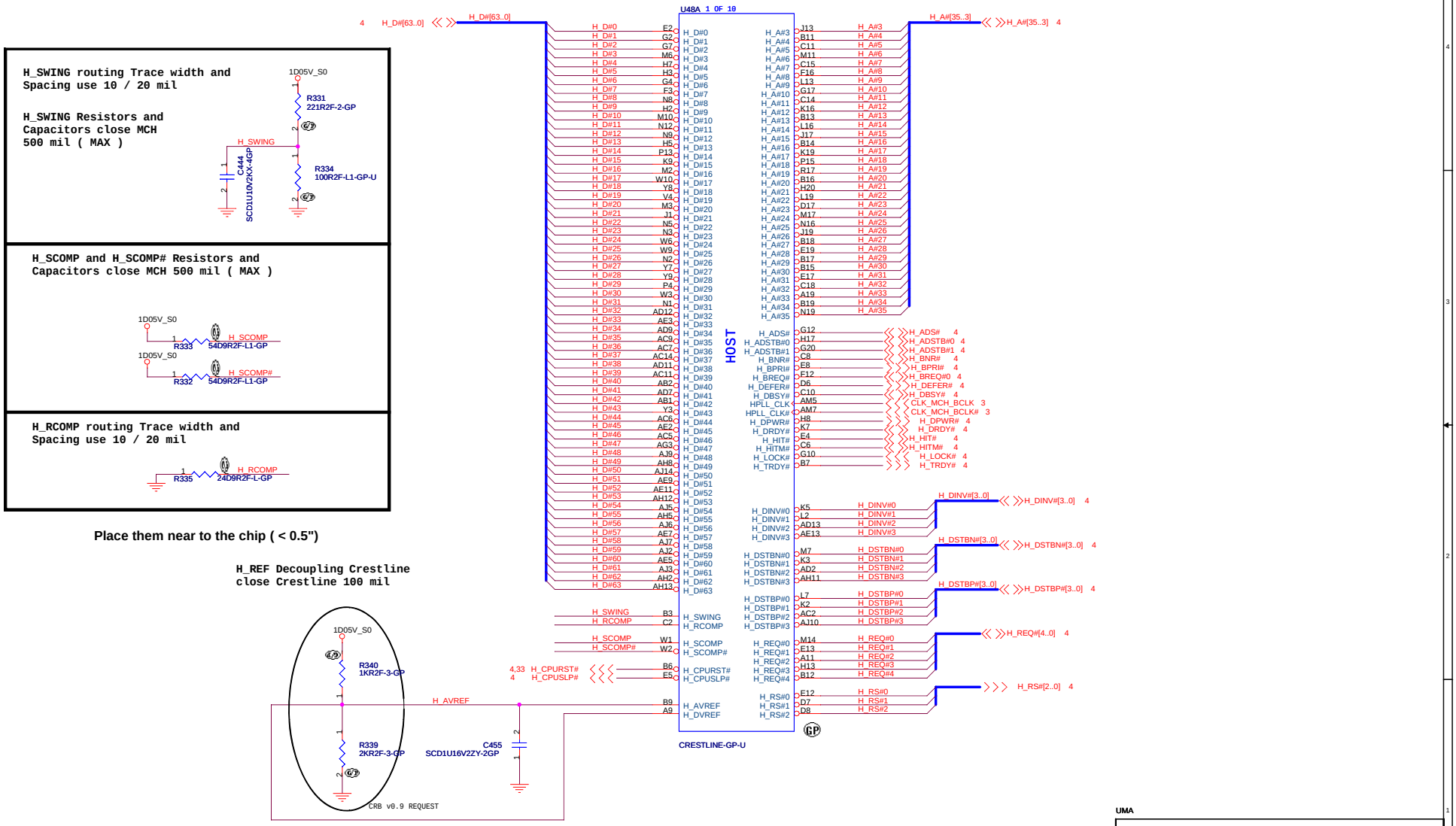

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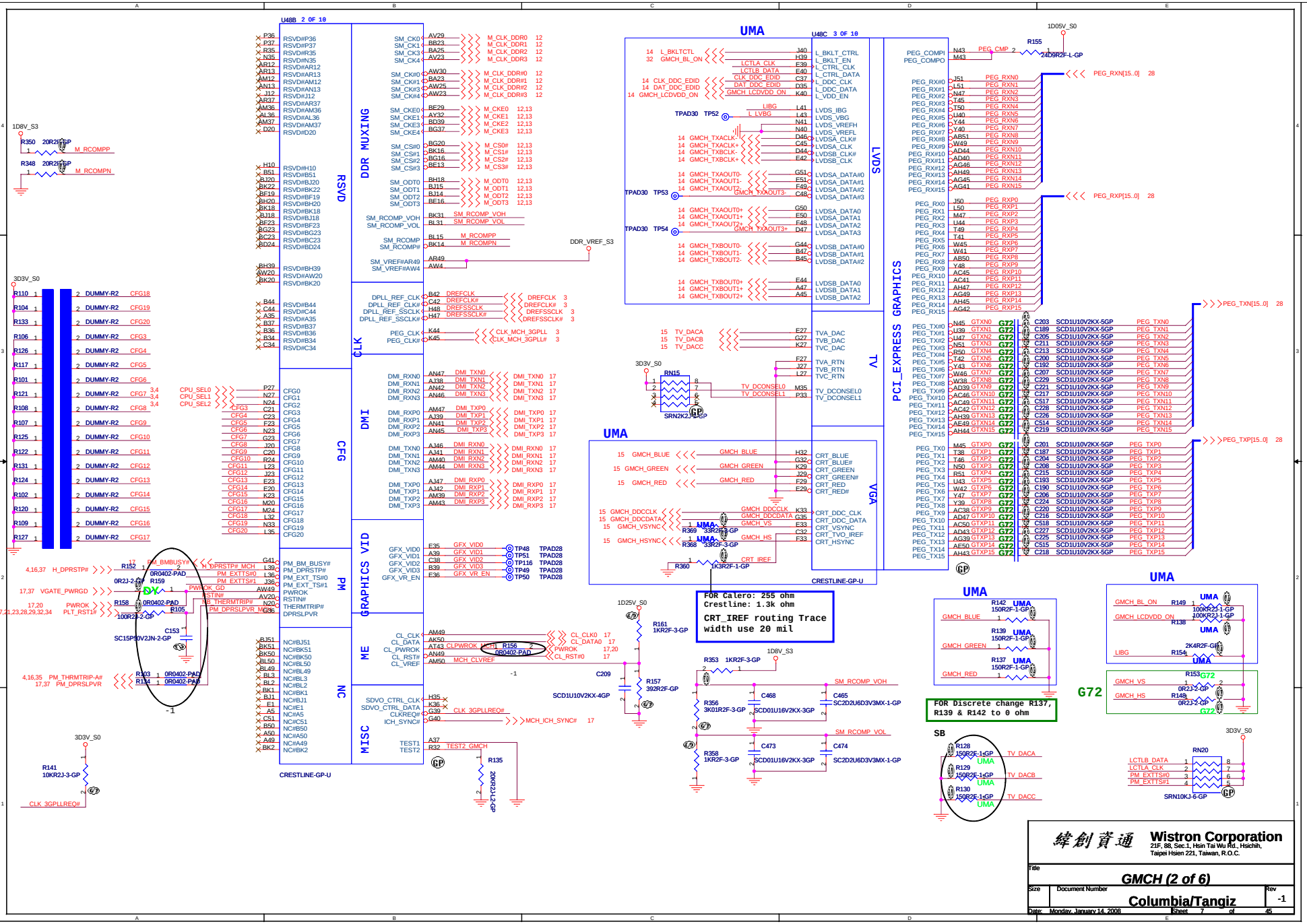
UMA
U48B 2 OF 10
U48C 3 OF 10
RSVD
DDR MUXING
CLK
CFG
DMI
PM
GRAPHICS VID
ME
NC
MISC
LVDS
TV
VGA
PCI_EXPRESS GRAPHICS
CRESTLINE-GP-U
FOR Calero: 255 ohm
Crestline: 1.3k ohm
CRT_IREF routing Trace width use 20 mil
FOR Discrete change R137, R139 & R142 to 0 ohm
SB
G72
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Title
GMCH (2 of 6)
Size
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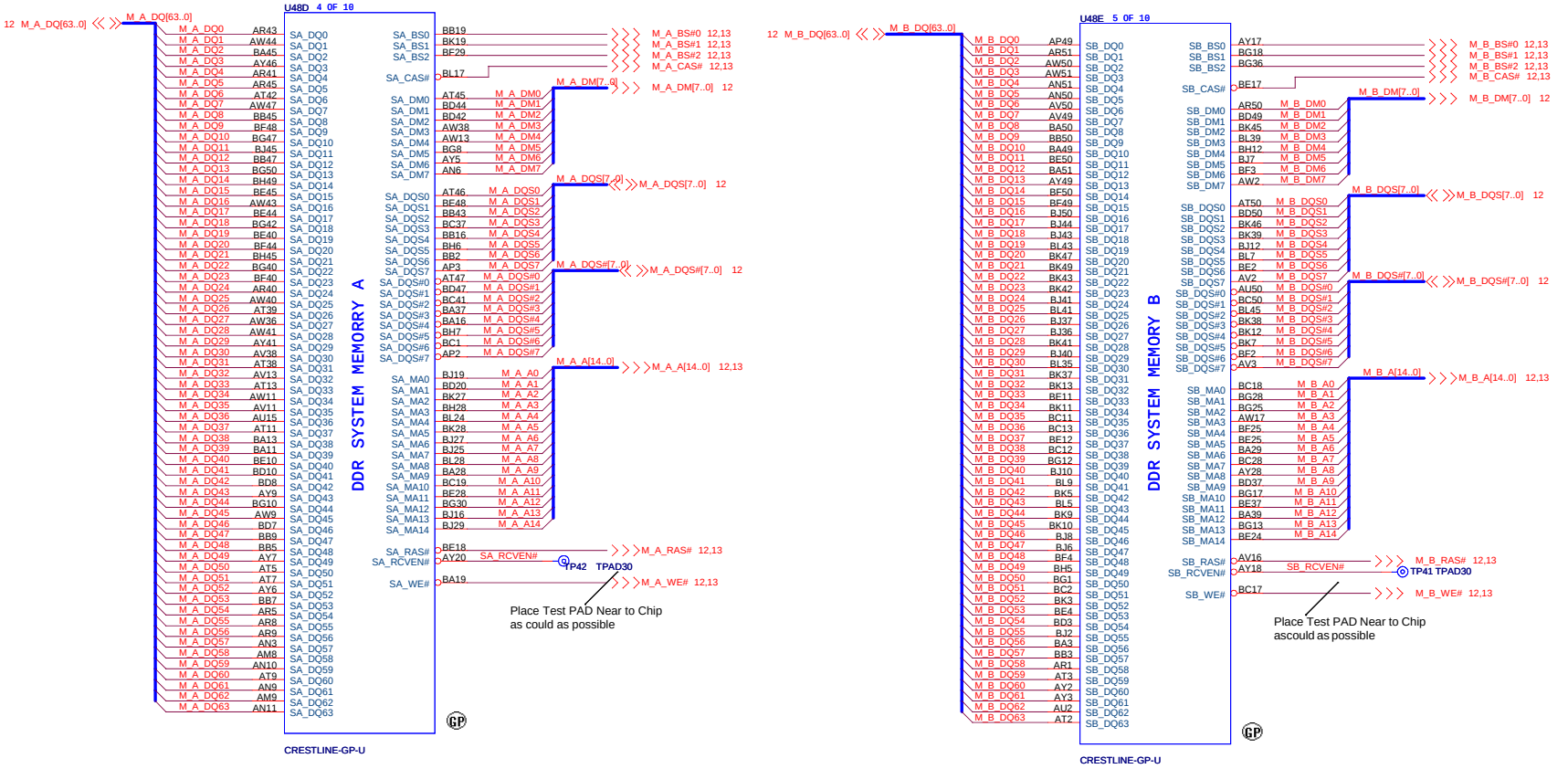

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Title: ***GMCH (3 of 6)***

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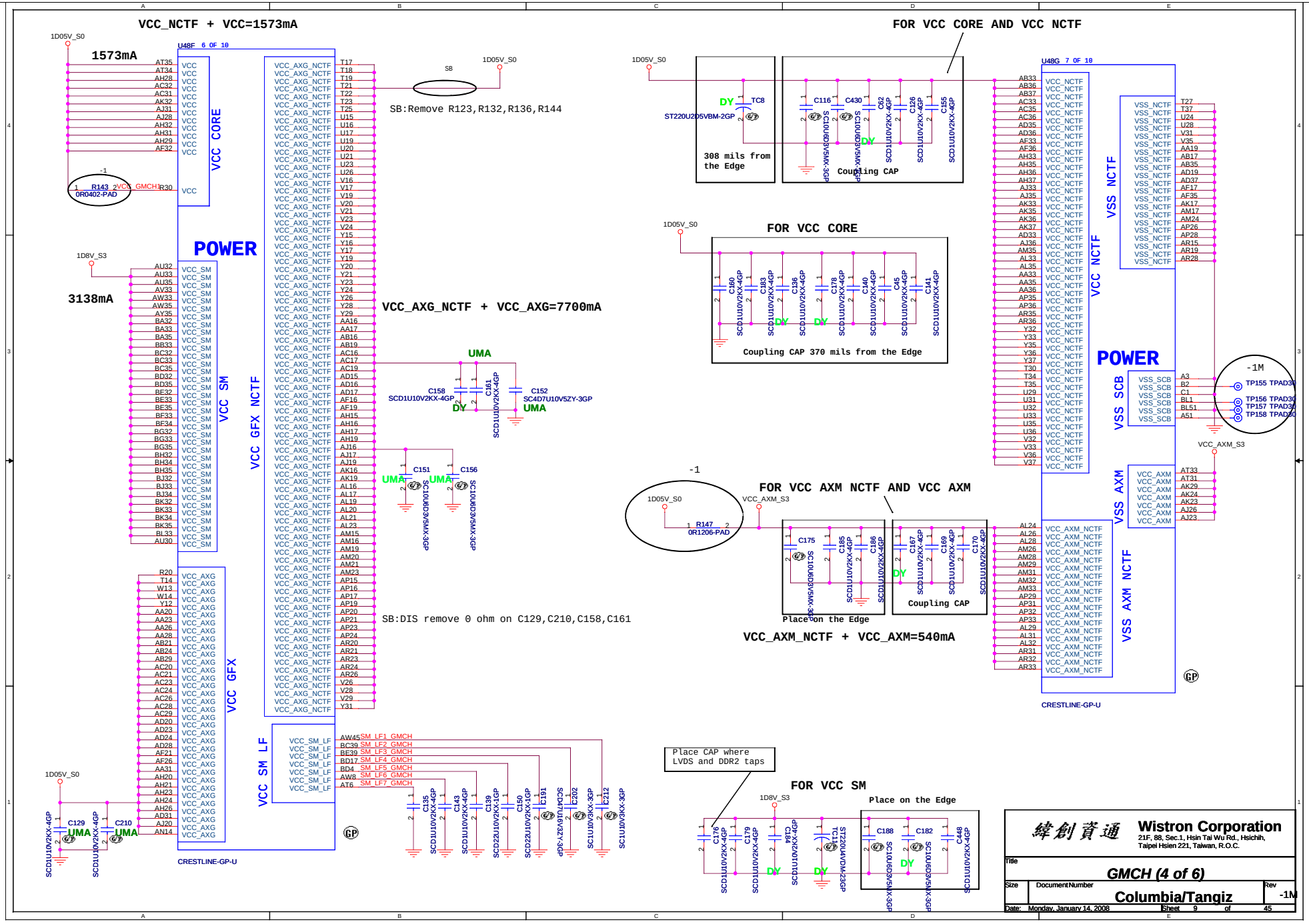
VCC_NCTF + VCC=1573mA
1573mA
1D05V_S0
U48F 6 OF 10
VCC CORE
POWER
R143 0R0402-PAD
VCC_GMCH
R30
1D8V_S3
3138mA
VCC_SM
VCC_GFX_NCTF
VCC_GFX
VCC_SM_LF
CRESTLINE-GP-U
SB
SB:Remove R123,R132,R136,R144
VCC_AXG_NCTF + VCC_AXG=7700mA
UMA
C158 SCD1U10V2KX-4GP
C161 SCD1U10V2KX-4GP
C152 SC4D7U10V5ZY-3GP
C151 SC10U6D3V5MX-3GP
C156 SC10U6D3V5MX-3GP
SB:DIS remove 0 ohm on C129,C210,C158,C161
C129 SCD1U10V2KX-4GP
C210 SCD1U10V2KX-4GP
SM_LF1_GMCH
SM_LF2_GMCH
SM_LF3_GMCH
SM_LF4_GMCH
SM_LF5_GMCH
SM_LF6_GMCH
SM_LF7_GMCH
C135 SCD1U10V2KX-4GP
C143 SCD1U10V2KX-4GP
C139 SCD22U10V2KX-1GP
C150 SCD22U10V2KX-1GP
C191 SCD47U6V3ZY-3GP
C202 SC1U10V3KX-3GP
C212 SC1U10V3KX-3GP
FOR VCC CORE AND VCC NCTF
1D05V_S0
DY TC8 ST220U2D5VBM-2GP
308 mils from the Edge
C116 SC10U6D3V5MX-3GP
C430 SC10U6D3V5MX-3GP
C62 SCD1U10V2KX-4GP
C126 SCD1U10V2KX-4GP
C155 SCD1U10V2KX-4GP
Coupling CAP
FOR VCC CORE
C160 SCD1U10V2KX-4GP
C183 SCD1U10V2KX-4GP
C136 SCD1U10V2KX-4GP
C178 SCD1U10V2KX-4GP
C140 SCD1U10V2KX-4GP
C45 SCD1U10V2KX-4GP
C141 SCD1U10V2KX-4GP
Coupling CAP 370 mils from the Edge
U48G 7 OF 10
VCC_NCTF
VSS_NCTF
VSS_SCB
VSS_AXM
VCC_AXM
VCC_AXM_NCTF
VSS_AXM_NCTF
POWER
-1M
TP155 TPAD30
TP156 TPAD30
TP157 TPAD30
TP158 TPAD30
VCC_AXM_S3
FOR VCC AXM NCTF AND VCC AXM
R147 0R1206-PAD
C175 SC10U6D3V5MX-3GP
C185 SCD1U10V2KX-4GP
C186 SCD1U10V2KX-4GP
C167 SCD1U10V2KX-4GP
C169 SCD1U10V2KX-4GP
C170 SCD1U10V2KX-4GP
Place on the Edge
Coupling CAP
VCC_AXM_NCTF + VCC_AXM=540mA
CRESTLINE-GP-U
Place CAP where LVDS and DDR2 taps
FOR VCC SM
1D8V_S3
Place on the Edge
C176 SCD1U10V2KX-4GP
C179 SCD1U10V2KX-4GP
C184 SCD1U10V2KX-4GP
TC11 ST220U4D0VDM-2GP
C188 SC10U6D3V5MX-3GP
C182 SC10U6D3V5MX-3GP
C448 SCD1U10V2KX-4GP
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Title
GMCH (4 of 6)
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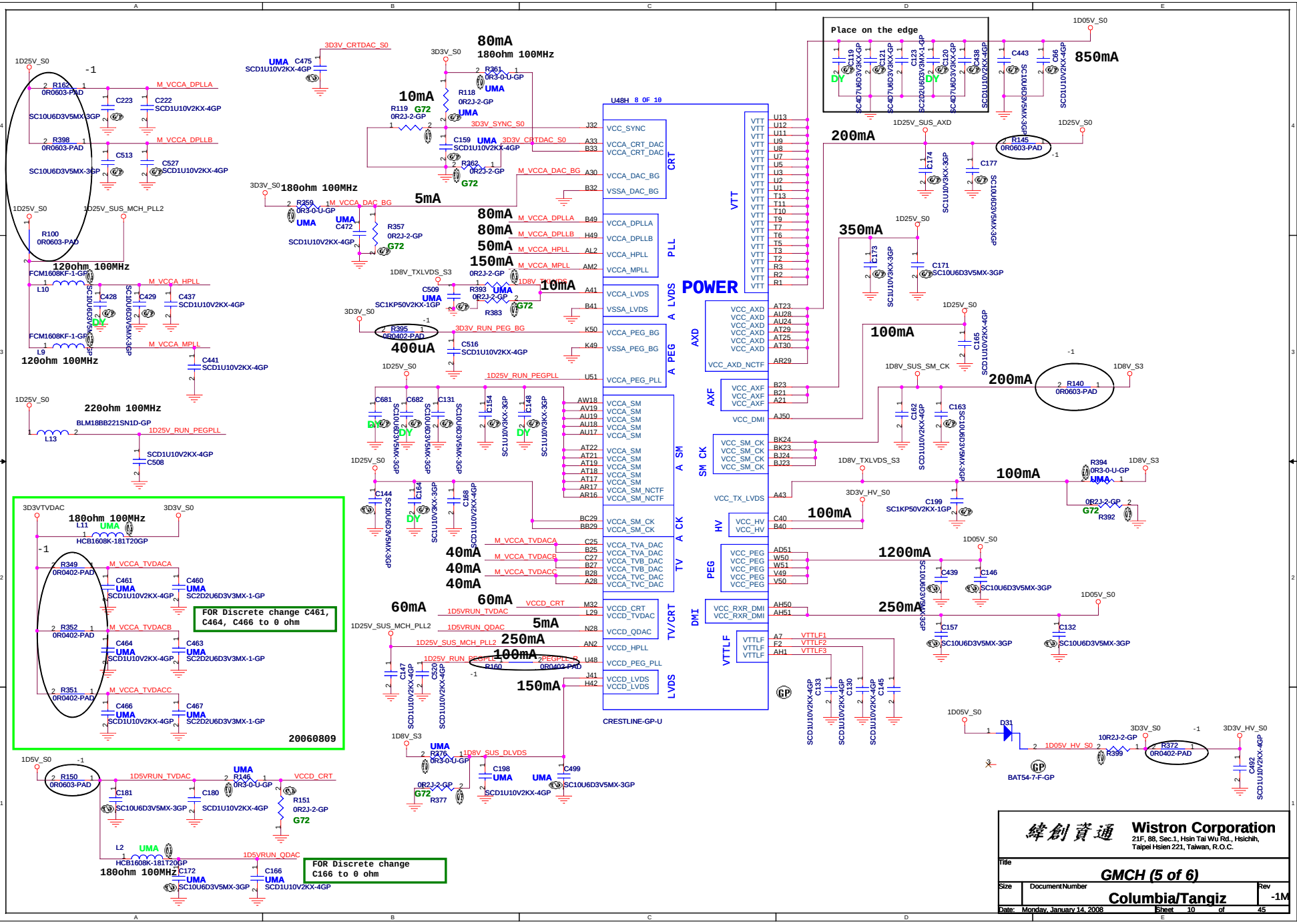
POWER
U48H 8 OF 10
CRESTLINE-GP-U
Place on the edge
FOR Discrete change C461, C464, C466 to 0 ohm
FOR Discrete change C166 to 0 ohm
20060809
850mA
200mA
350mA
100mA
200mA
100mA
100mA
1200mA
250mA
80mA
180ohm 100MHz
10mA
5mA
80mA
80mA
50mA
150mA
10mA
400uA
120ohm 100MHz
220ohm 100MHz
40mA
40mA
40mA
60mA
60mA
5mA
250mA
100mA
150mA
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GMCH (5 of 6)
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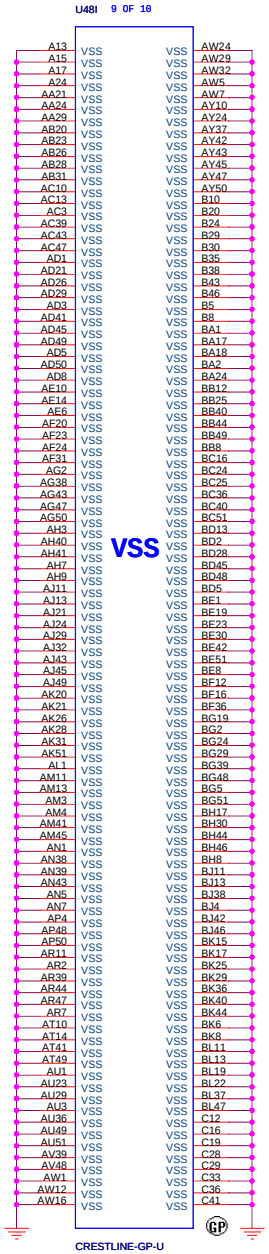

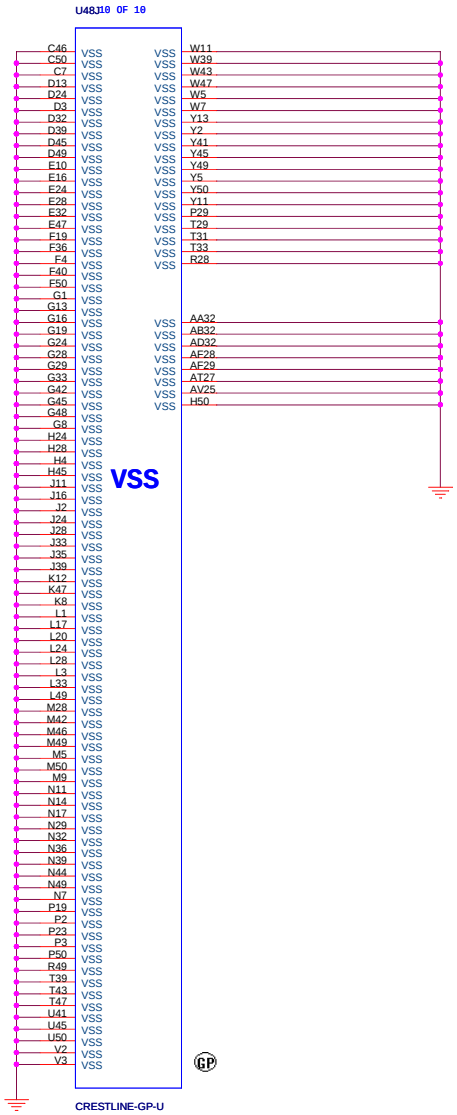

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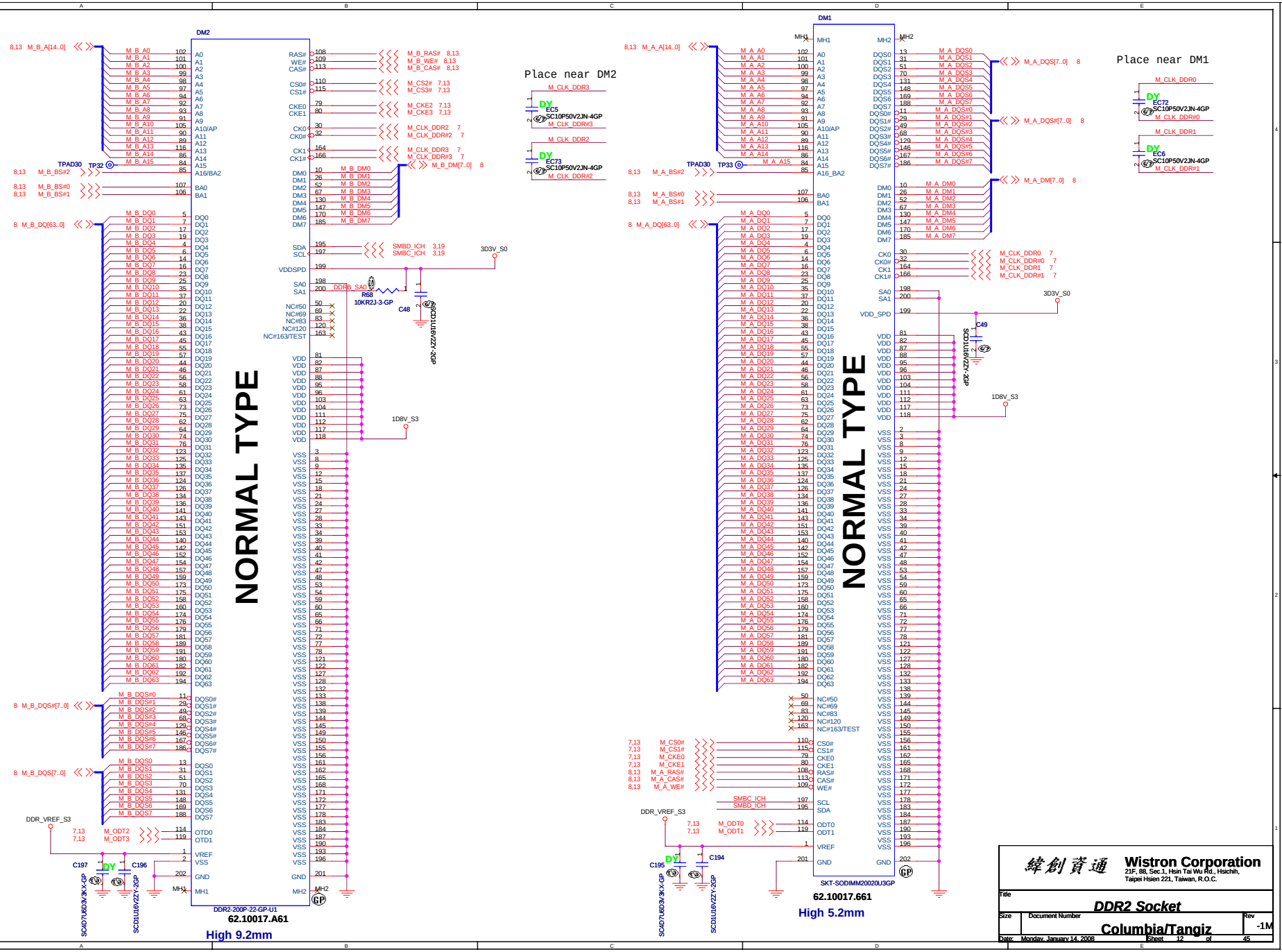
DM2
NORMAL TYPE
DDR2-200P-22-GP-U1
62.10017.A61
High 9.2mm
Place near DM2
DM1
NORMAL TYPE
SKT-SODIMM20020U3GP
62.10017.661
High 5.2mm
Place near DM1
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DDR2 Socket
Columbia/Tangiz
-1M
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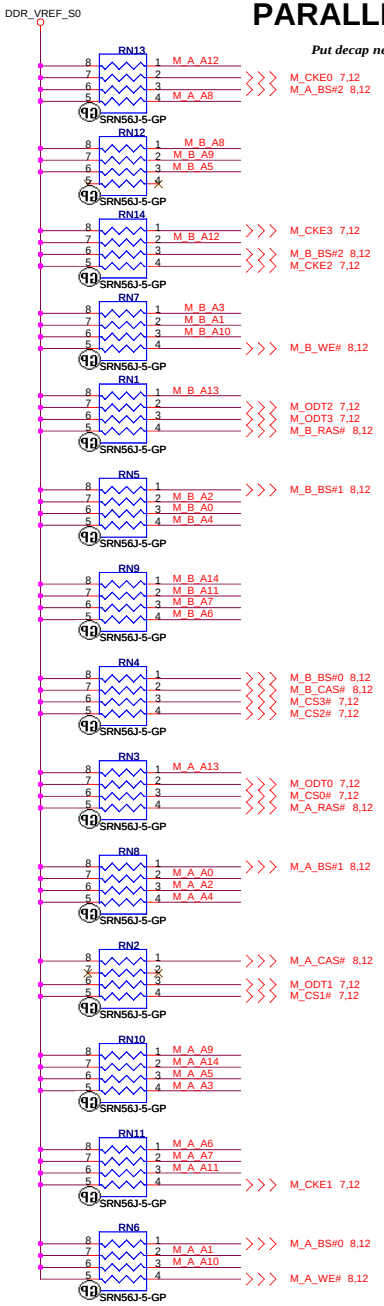
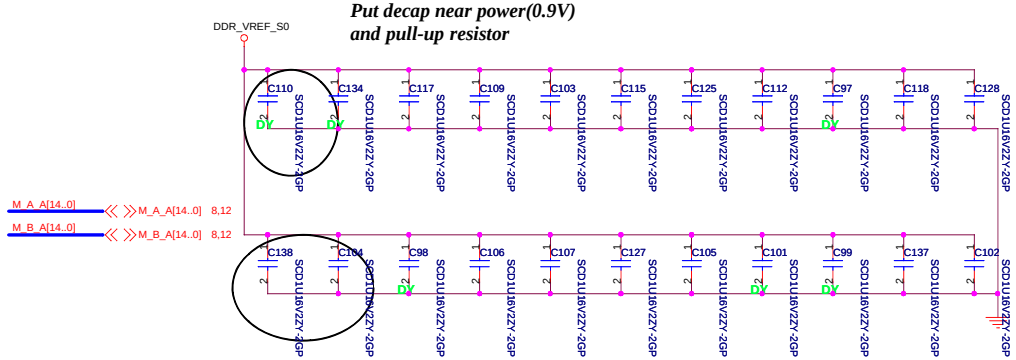
PARALLEL TERMINATION

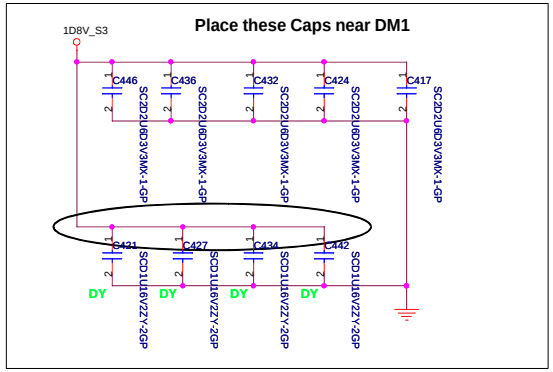
Put decap near power(0.9V) and pull-up resistor

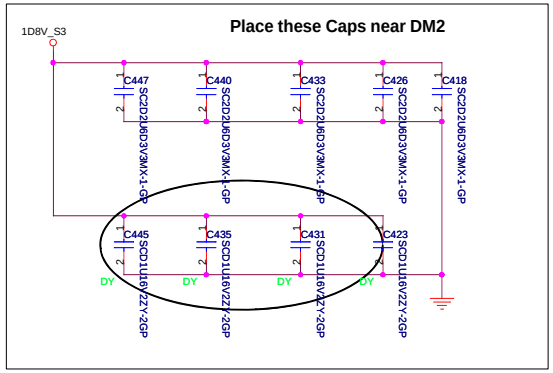


Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor







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Title: ***DDR2 Termination Resistor***

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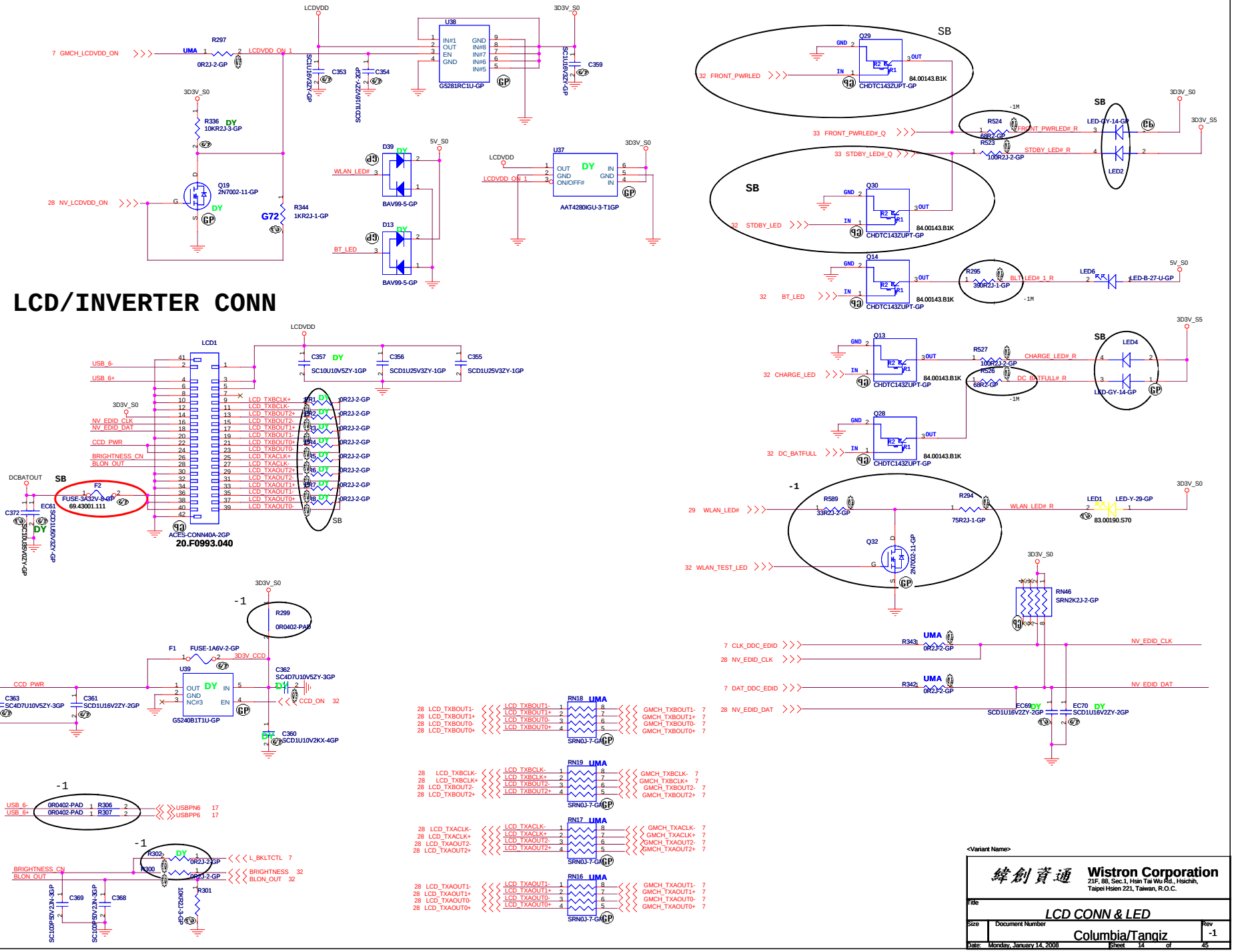
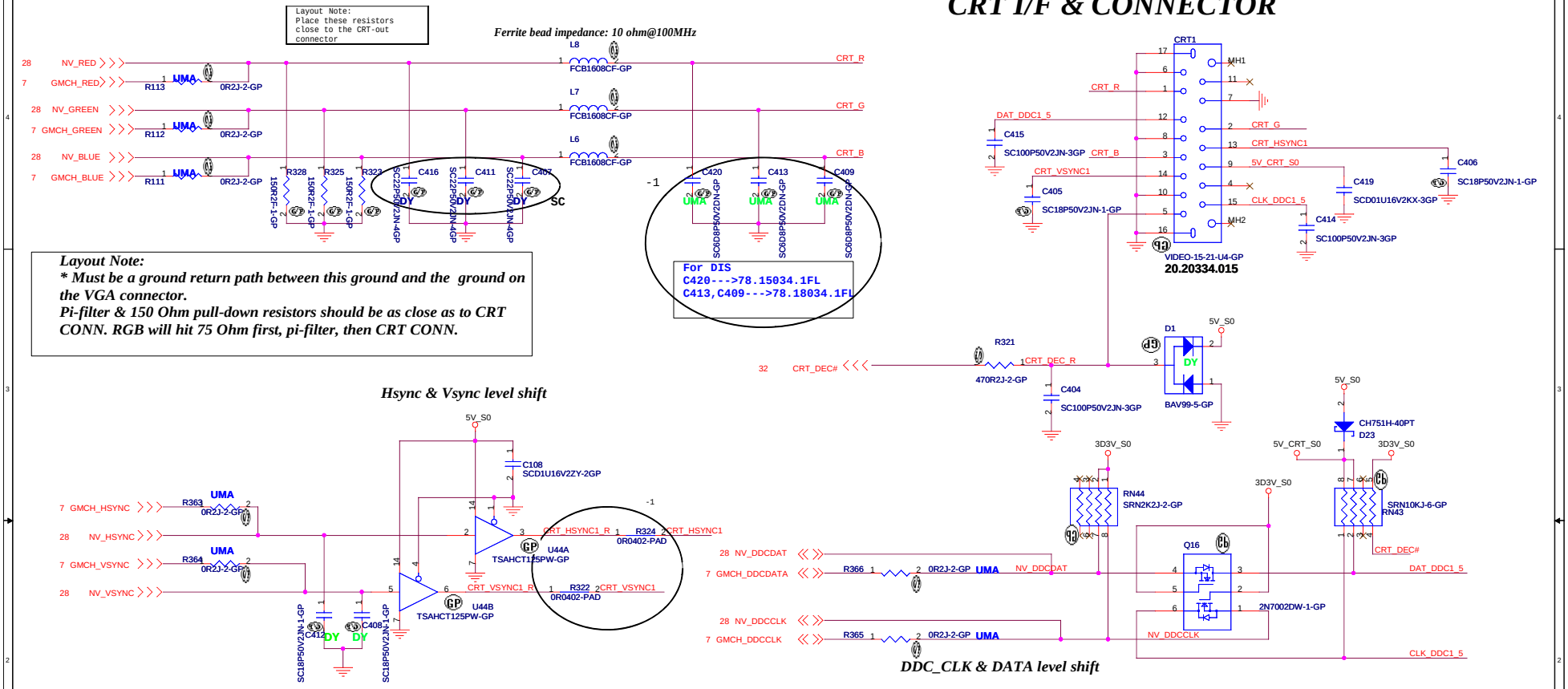
LCD/INVERTER CONN



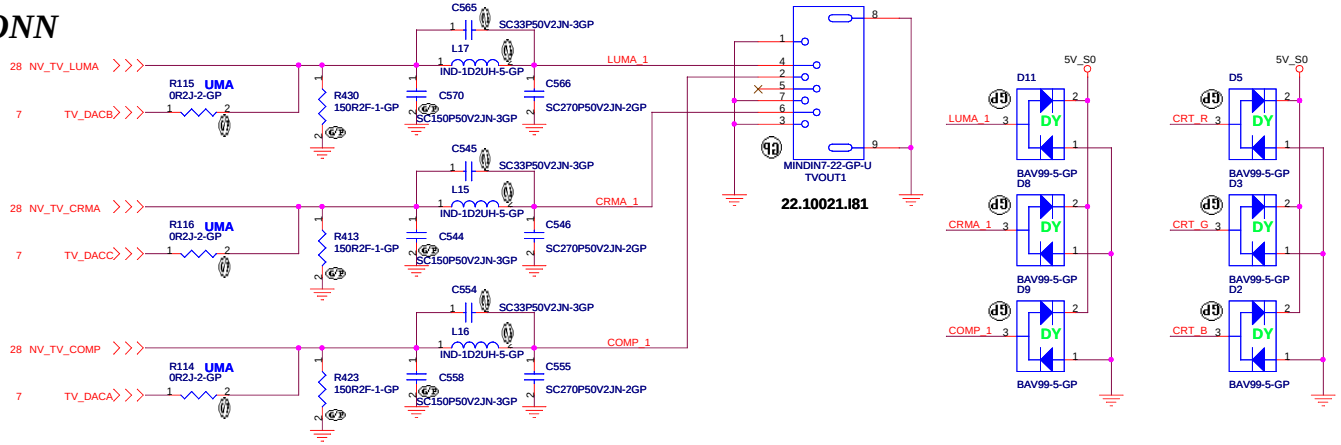
<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	*LCD CONN & LED*
Size / Document Number	Columbia/Tangiz
Rev	-1
Date: Monday, January 14, 2008	Sheet 14 of 45

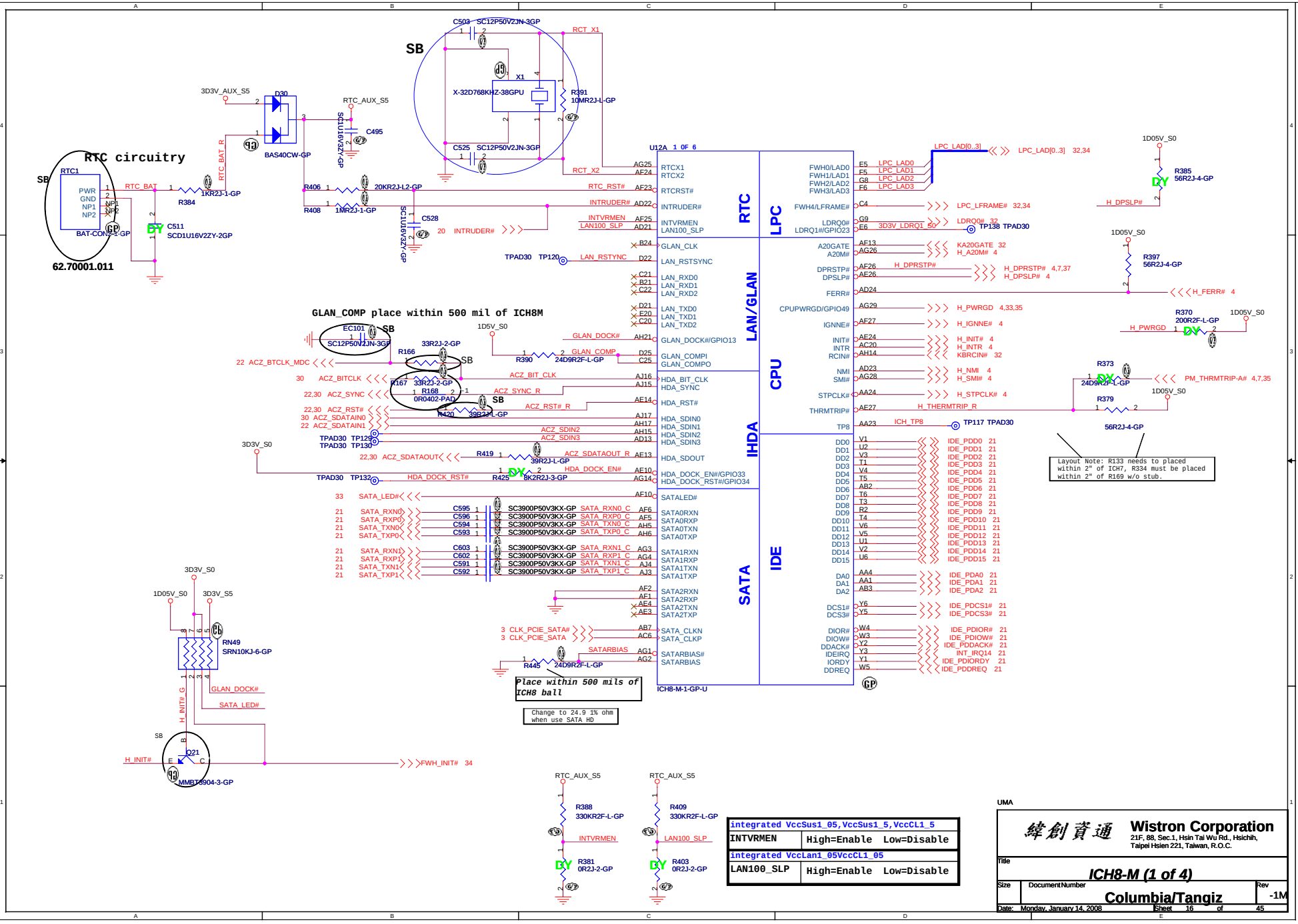
CRT I/F & CONNECTOR



TV CONN



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	CRT/TV Connector	
Size	Document Number: Columbia/Tangiz	Rev: -1
Date: Monday, January 14, 2008	Sheet 15 of 45	


RTC circuitry
62.70001.011
GLAN_COMP place within 500 mil of ICH8M
U12A 1 0F 6
RTC
LPC
LAN/GLAN
CPU
IHDA
SATA
IDE
ICH8-M-1-GP-U
Place within 500 mils of ICH8 ball
Change to 24.9 1% ohm when use SATA HD
Layout Note: R133 needs to placed within 2" of ICH7, R334 must be placed within 2" of R169 w/o stub.
integrated VccSus1_05,VccSus1_5,VccCL1_5
INTVRMEN High=Enable Low=Disable
integrated VccLan1_05VccCL1_05
LAN100_SLP High=Enable Low=Disable
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH8-M (1 of 4)
Size
Document Number
Columbia/Tangiz
Rev
-1M
Date: Monday, January 14, 2008
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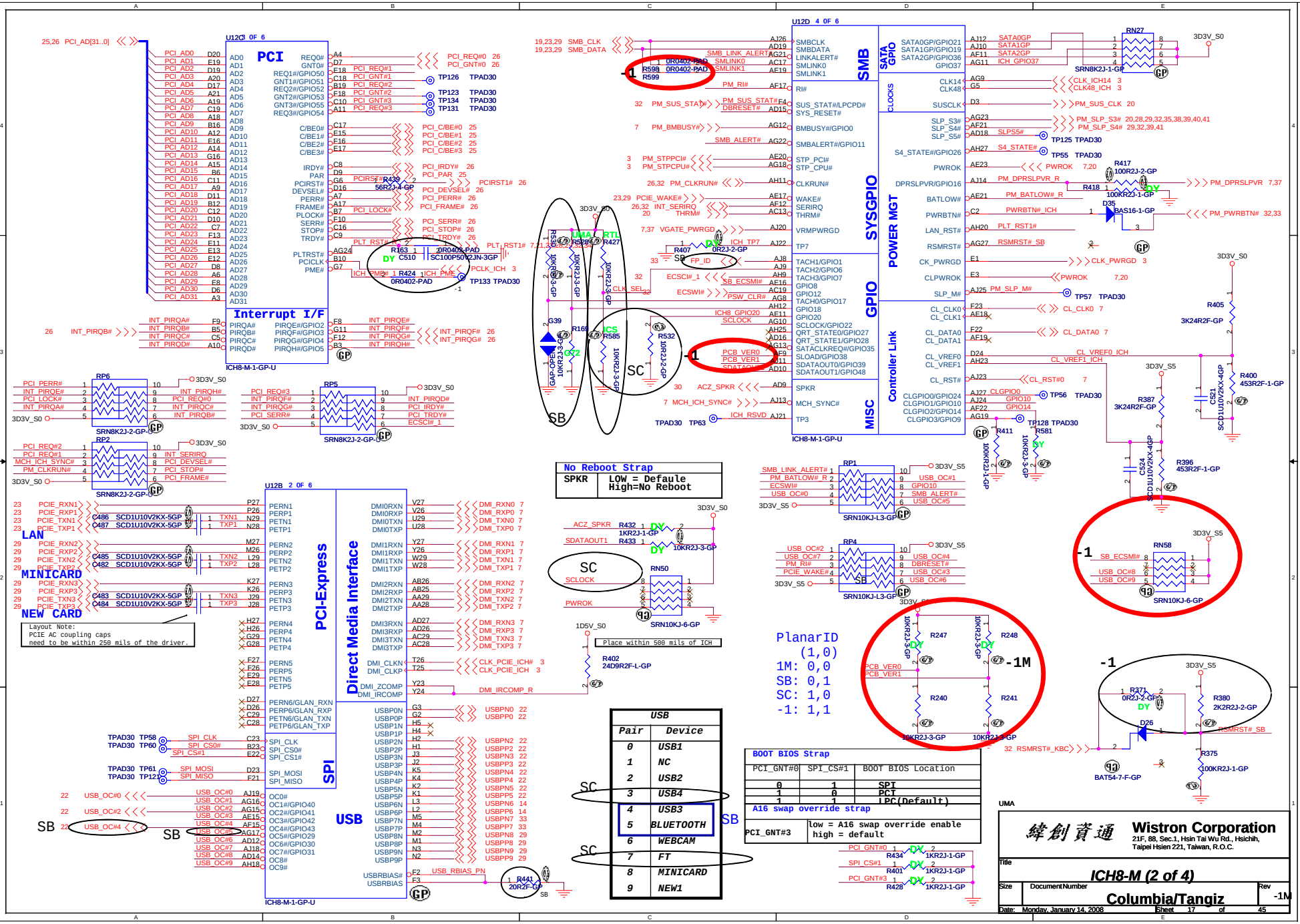
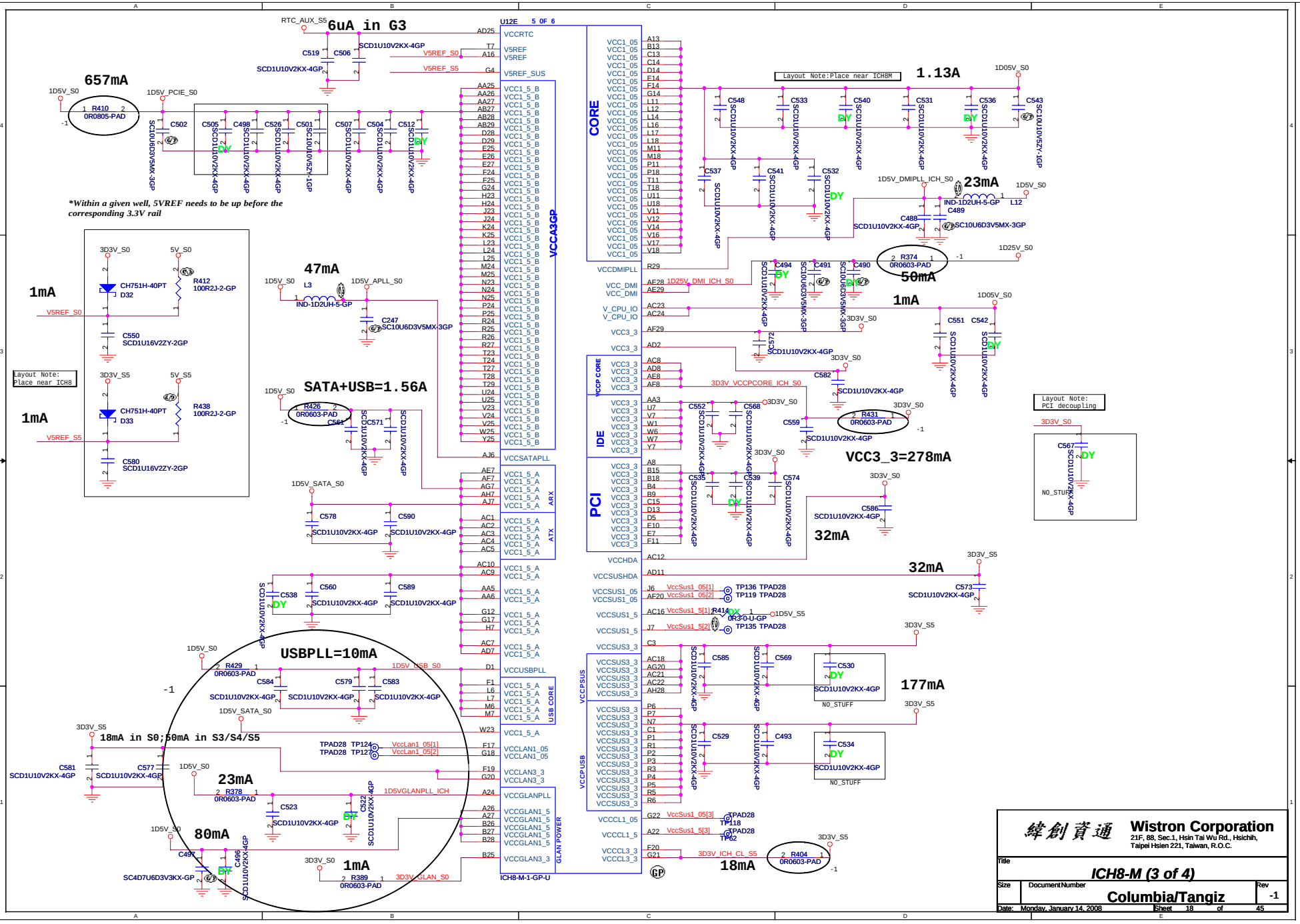

PCI
Interrupt I/F
ICH8-M-1-GP-U
SMB
SATA GPIO
CLOCKS
SYSGPIO
POWER MGT
GPIO
Controller Link
MISC
Direct Media Interface
PCI-Express
SPI
USB
LAN
MINICARD
NEW CARD
SB
SC
UMA
RTL
No Reboot Strap
SPKR LOW = Defaule
High=No Reboot
Layout Note:
PCIE AC coupling caps
need to be within 250 mils of the driver.
Place within 500 mils of ICH
PlanarID
(1,0)
1M: 0,0
SB: 0,1
SC: 1,0
-1: 1,1
USB
Pair Device
0 USB1
1 NC
2 USB2
3 USB4
4 USB3
5 BLUETOOTH
6 WEBCAM
7 FT
8 MINICARD
9 NEW1
BOOT BIOS Strap
PCI_GNT#0 SPI_CS#1 BOOT BIOS Location
0 1 SPI
1 0 PCI
1 1 LPC(Default)
A16 swap override strap
PCI_GNT#3 low = A16 swap override enable
high = default
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH8-M (2 of 4)
Size
Document Number
Columbia/Tangiz
Rev
-1M
Date: Monday, January 14, 2008
Sheet 17 of 45


6uA in G3
657mA
1.13A
23mA
50mA
1mA
47mA
SATA+USB=1.56A
VCC3_3=278mA
32mA
177mA
USBPLL=10mA
18mA in S0;50mA in S3/S4/S5
23mA
80mA
18mA
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
Layout Note:Place near ICH8M
Layout Note: Place near ICH8
Layout Note: PCI decoupling
U12E 5 OF 6
CORE
IDE
PCI
VCCA3GP
ICH8-M-1-GP-U
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
ICH8-M (3 of 4)
Columbia/Tangiz
Date: Monday, January 14, 2008
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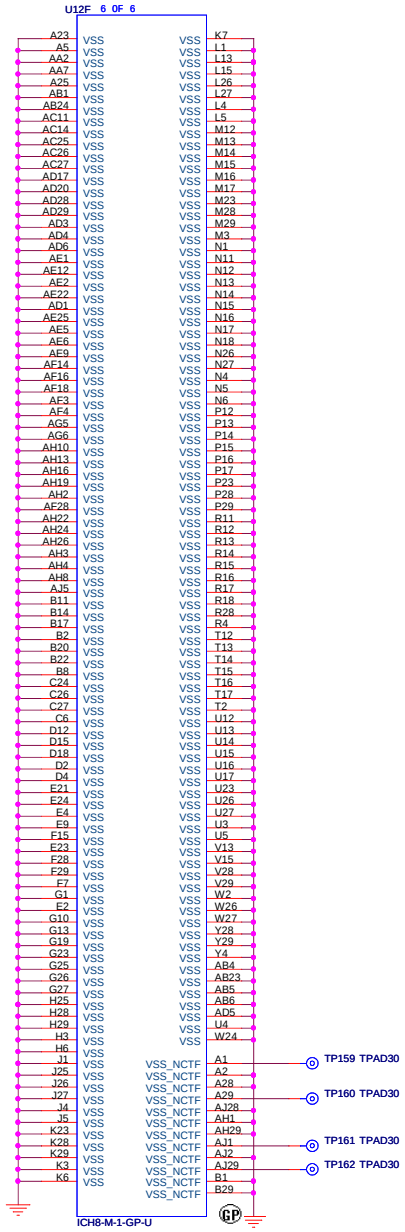

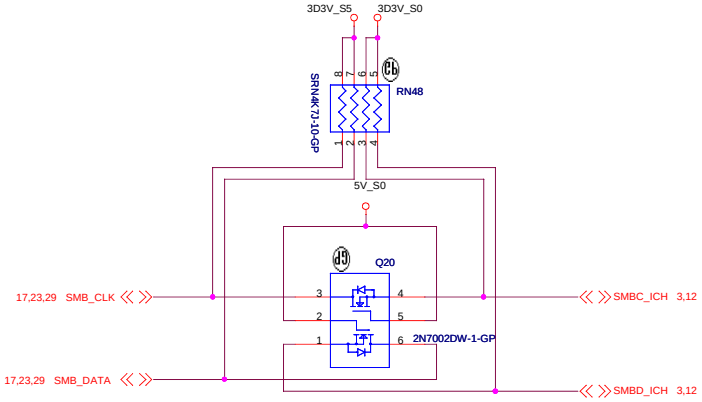

Q13 & Q14 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance

SMBUS

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	***ICH8-M (4 of 4)***		
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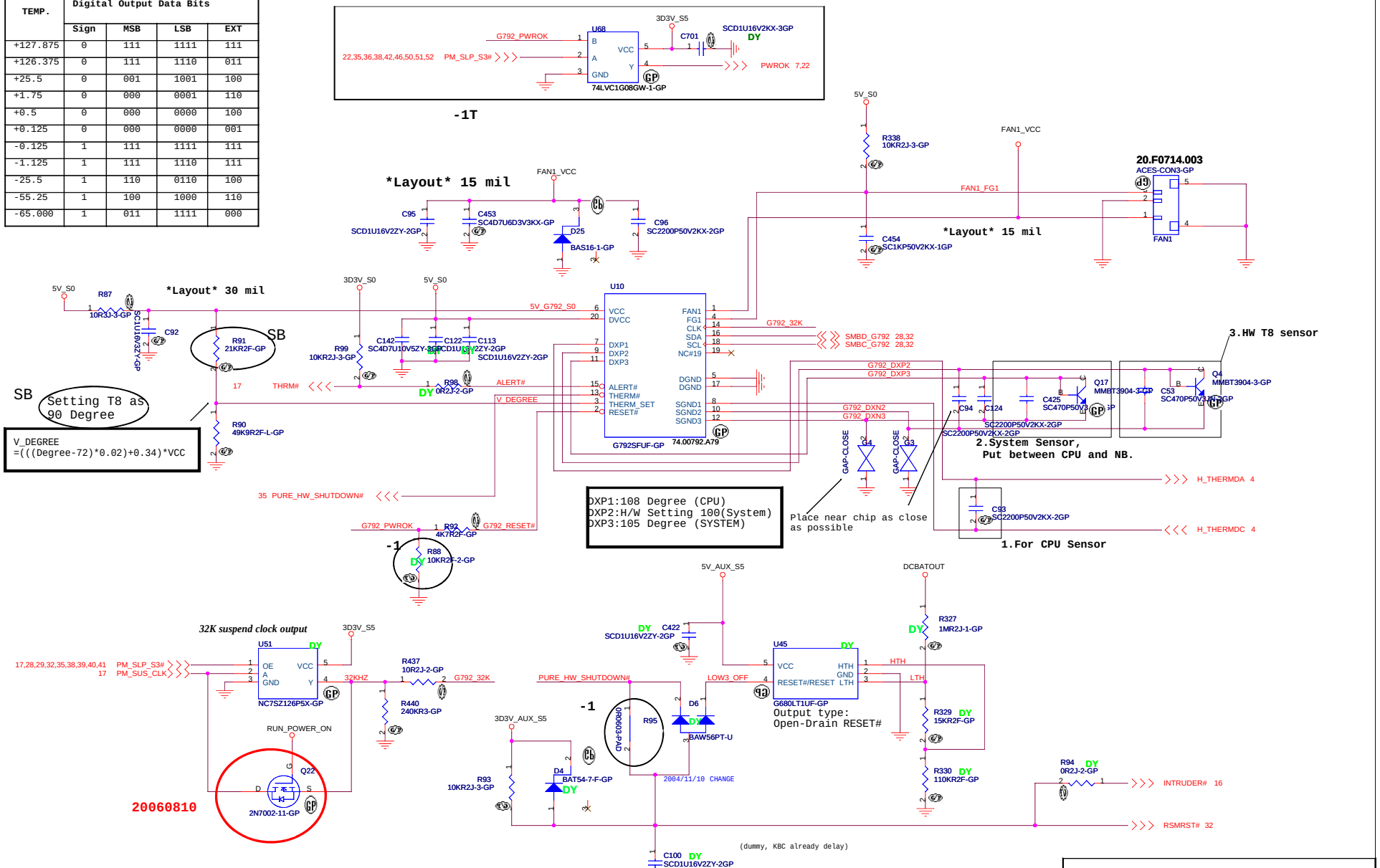
TEMP.	Digital Output Data Bits			
	Sign	MSB	LSB	EXT
+127.875	0	111	1111	111
+126.375	0	111	1110	011
+25.5	0	001	1001	100
+1.75	0	000	0001	110
+0.5	0	000	0000	100
+0.125	0	000	0000	001
-0.125	1	111	1111	111
-1.125	1	111	1110	111
-25.5	1	110	0110	100
-55.55	1	100	1000	110
-65.000	1	011	1111	000



緯創資通 Wistron Corporation
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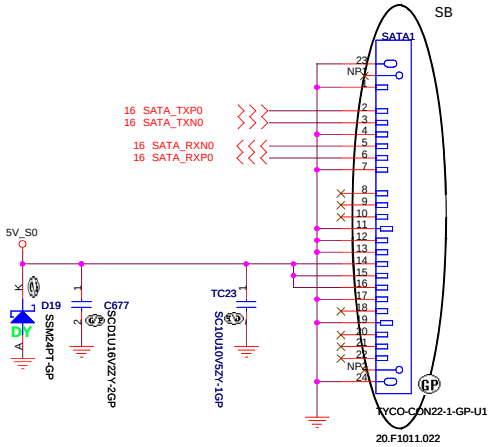
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor

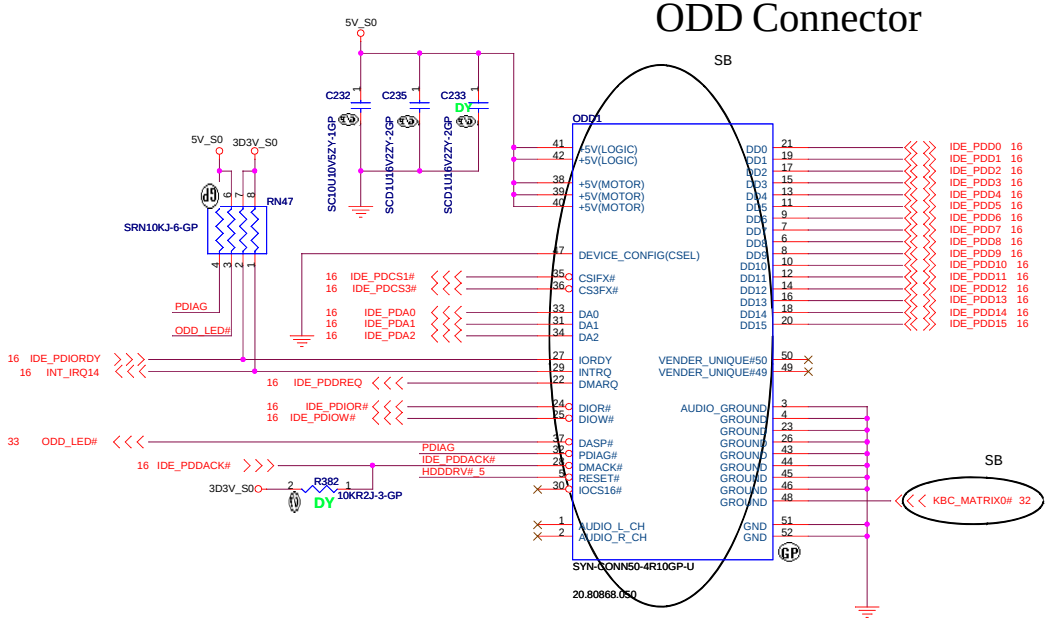
Size | Document Number: Columbia/Tangiz | Rev: -1M

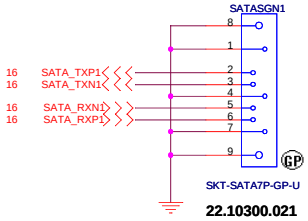
Date: Monday, January 14, 2008 | Sheet 20 of 45

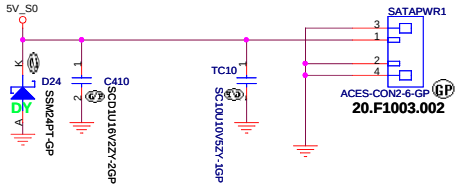
SATA HD Connector

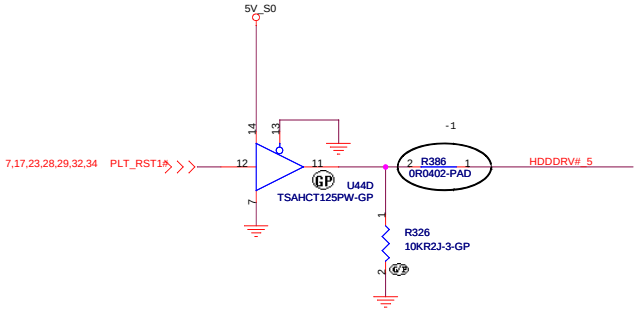


ODD Connector









bom1

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***HDD and CDROM***	
Size	Document Number **Columbia/Tangiz**	Rev -1M
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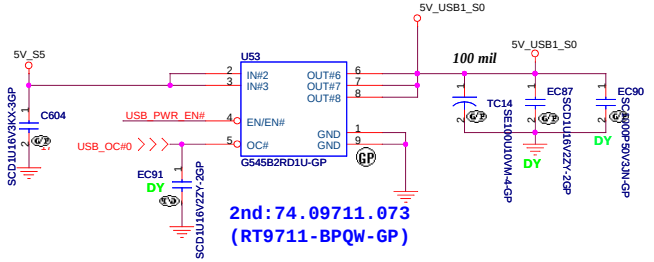
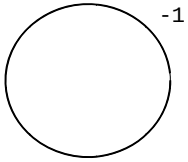
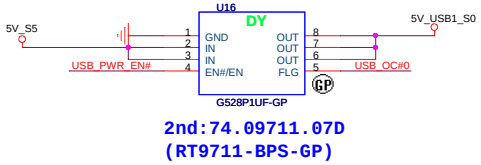
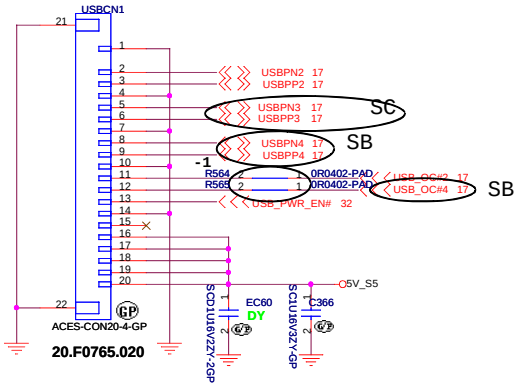
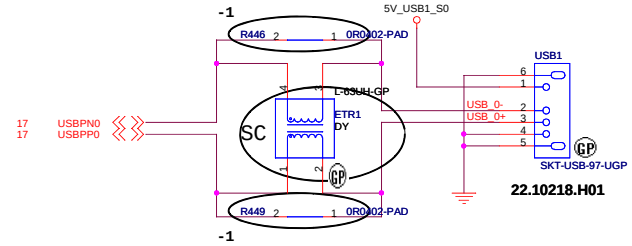


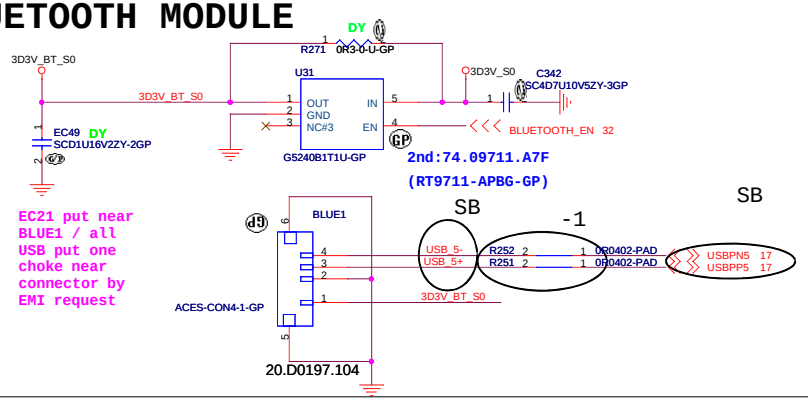






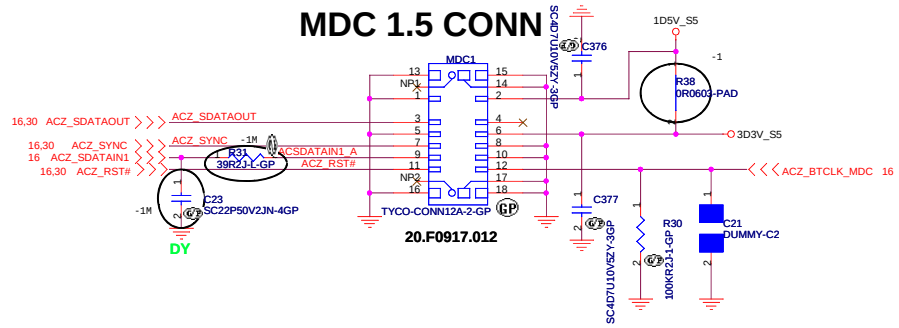


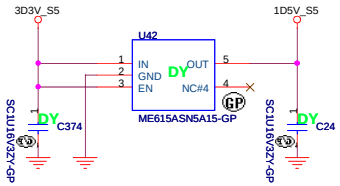
BLUETOOTH MODULE



EC21 put near BLUE1 / all USB put one choke near connector by EMI request

MDC 1.5 CONN





bom1

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	USB / MDC / BLUETOOTH	
Size	Document Number: Columbia/Tangiz	Rev: -1M
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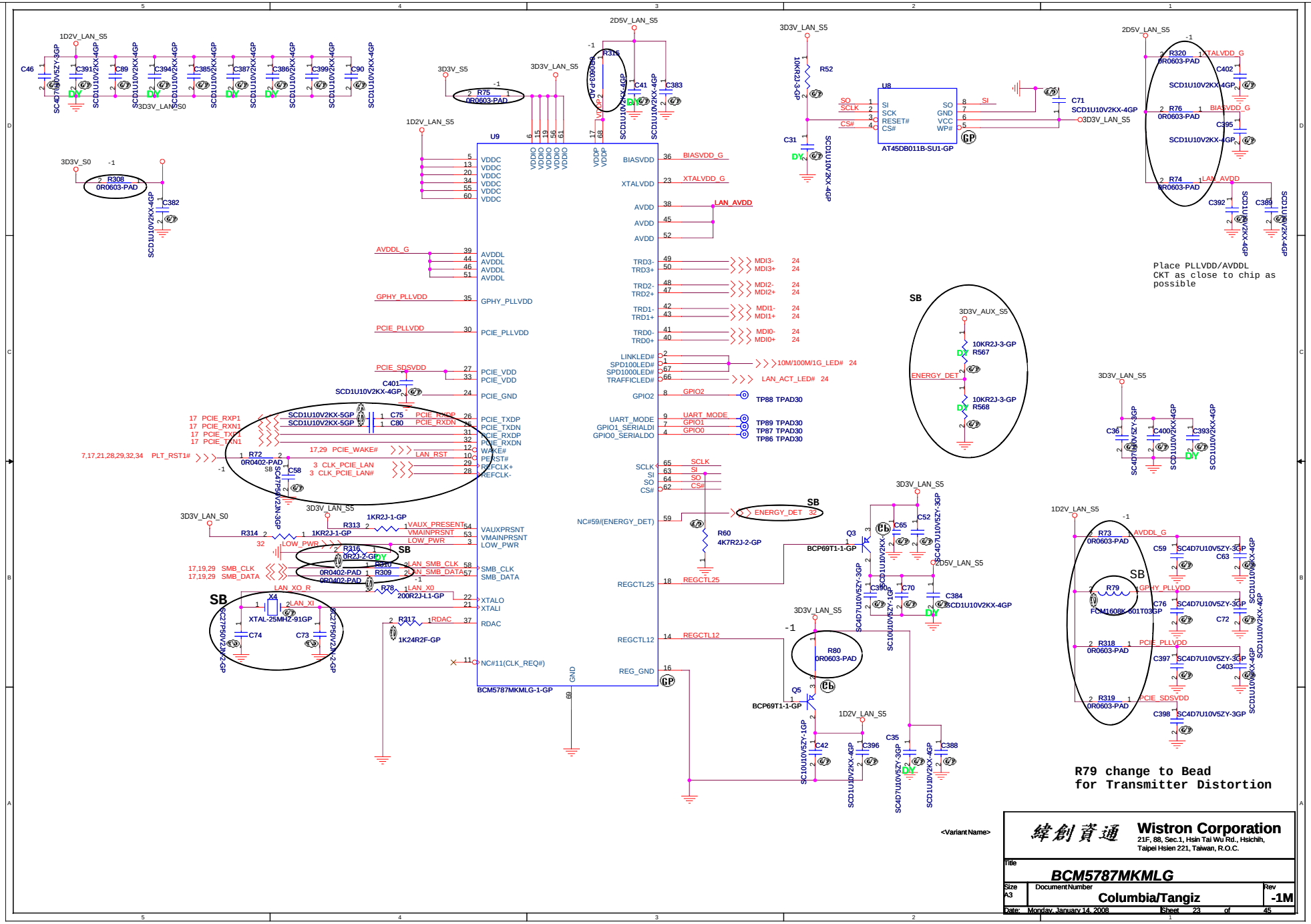
U9
BCM5787MKMLG-1-GP
U8
AT45DB011B-SU1-GP
Place PLLVDD/AVDDL CKT as close to chip as possible
R79 change to Bead for Transmitter Distortion
SB
DY
GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
BCM5787MKMLG
Size A3
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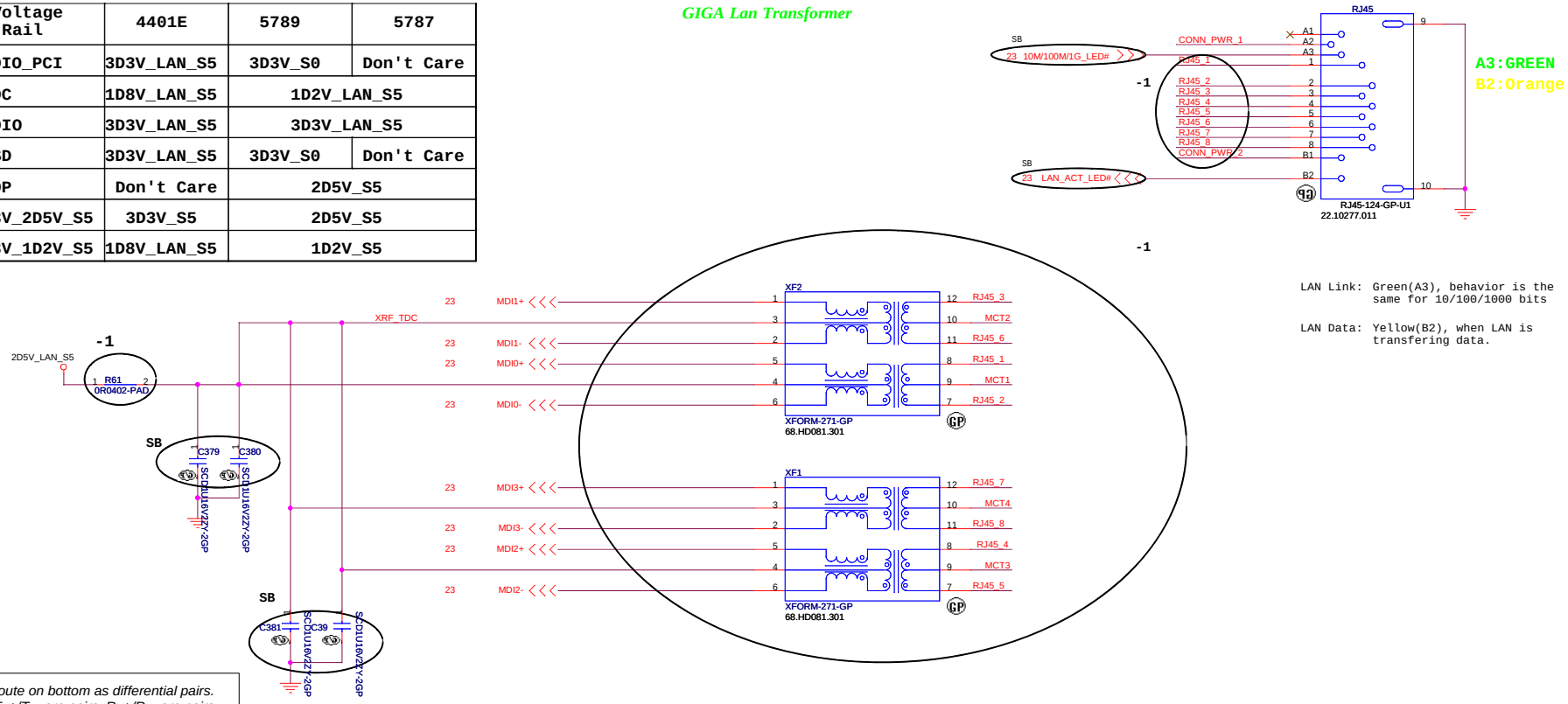
LAN Connector

Voltage Rail	4401E	5789	5787
VDDIO_PCI	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDC	1D8V_LAN_S5	1D2V_LAN_S5	
VDDIO	3D3V_LAN_S5	3D3V_LAN_S5	
VESD	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDP	Don't Care	2D5V_S5	
3D3V_2D5V_S5	3D3V_S5	2D5V_S5	
1D8V_1D2V_S5	1D8V_LAN_S5	1D2V_S5	

GIGA Lan Transformer



LAN Link: Green(A3), behavior is the same for 10/100/1000 bits

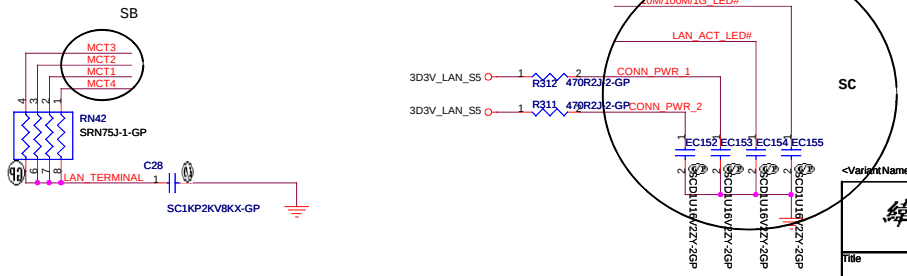
LAN Data: Yellow(B2), when LAN is transfering data.

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

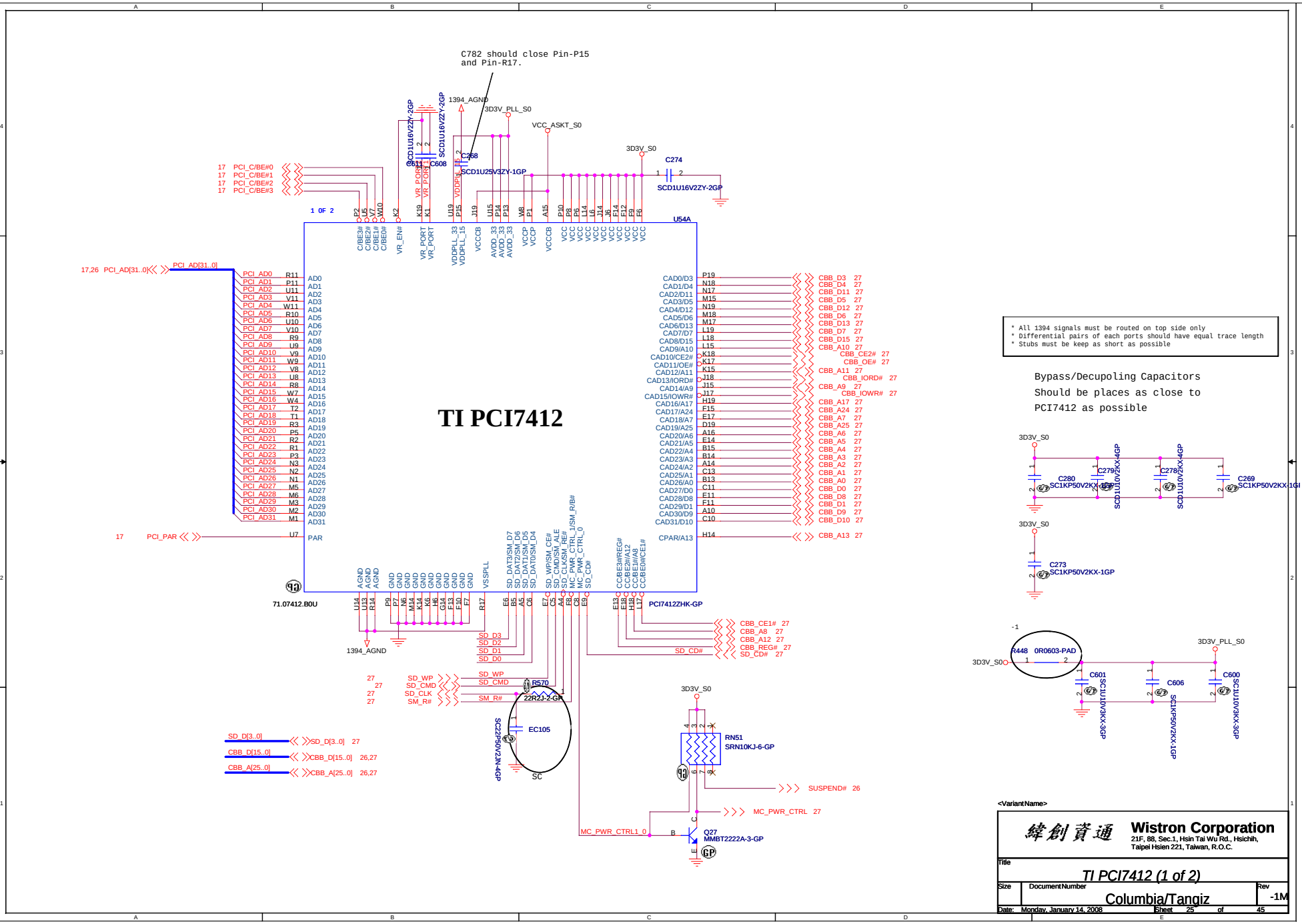
DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6



CLOSE TO TRANSFORMER

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.


C782 should close Pin-P15
and Pin-R17.
TI PCI7412
U54A
1 OF 2
PCI7412ZHK-GP
71.07412.B0U
* All 1394 signals must be routed on top side only
* Differential pairs of each ports should have equal trace length
* Stubs must be keep as short as possible
Bypass/Decupoling Capacitors
Should be places as close to
PCI7412 as possible
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
TI PCI7412 (1 of 2)
Columbia/Tangiz
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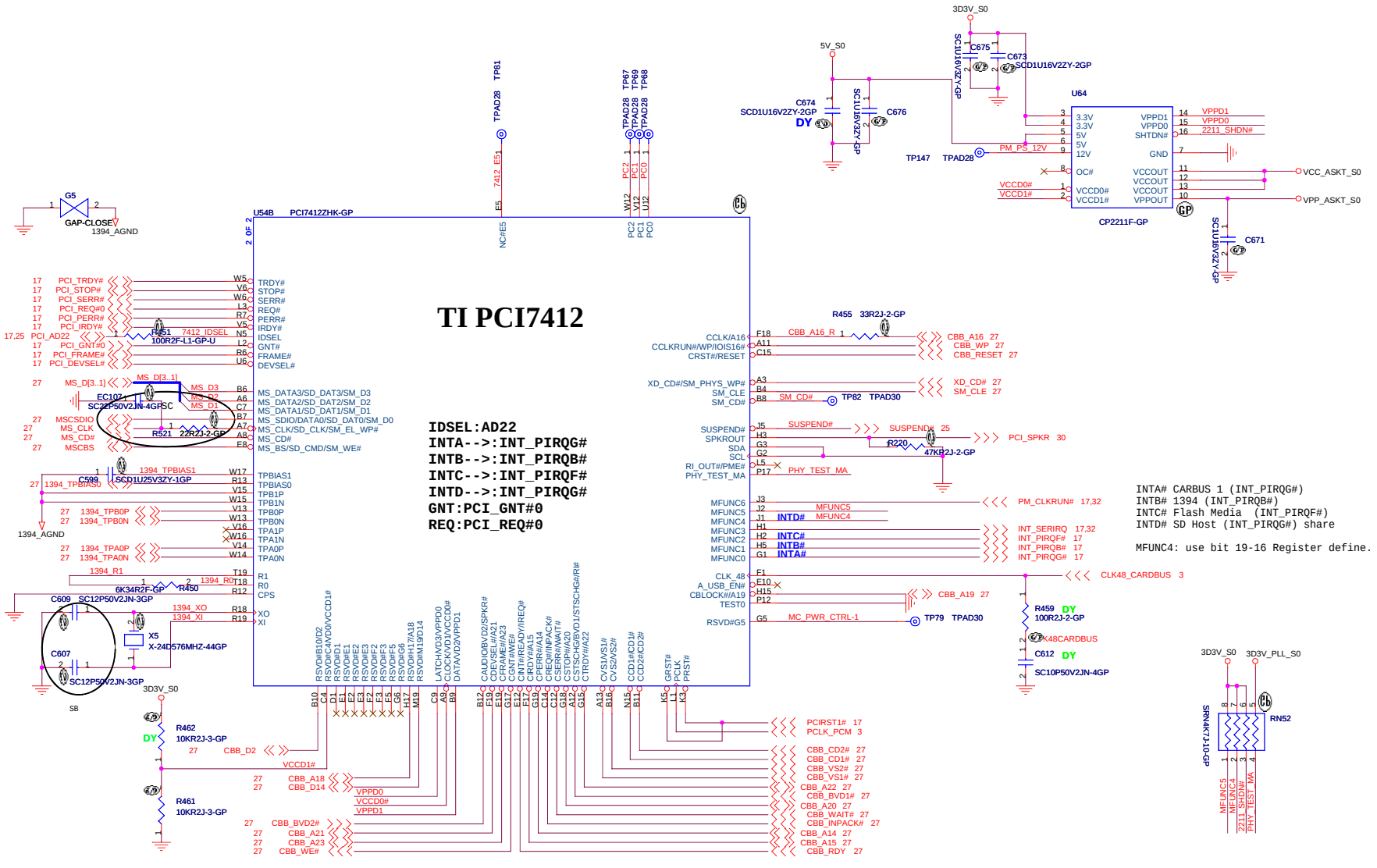

Wistron Corporation
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Title: TI PCI7412 (2 of 2)

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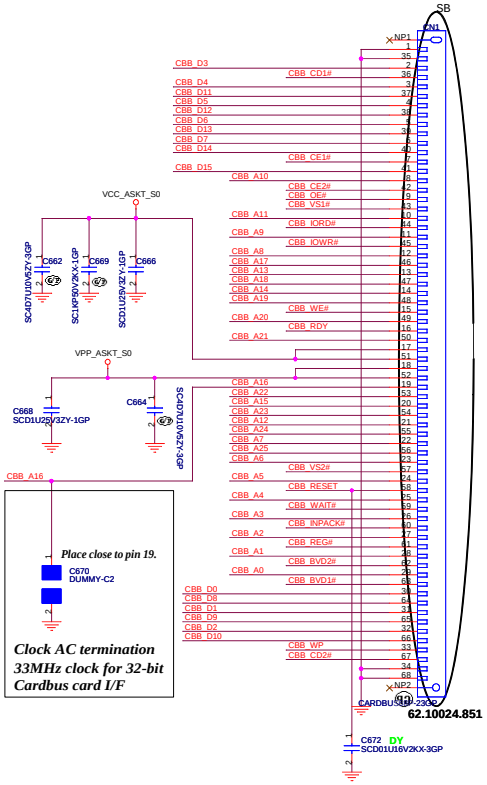
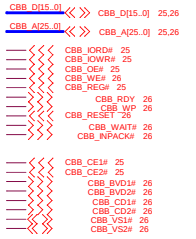
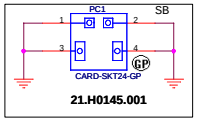
PCMCIA Socket

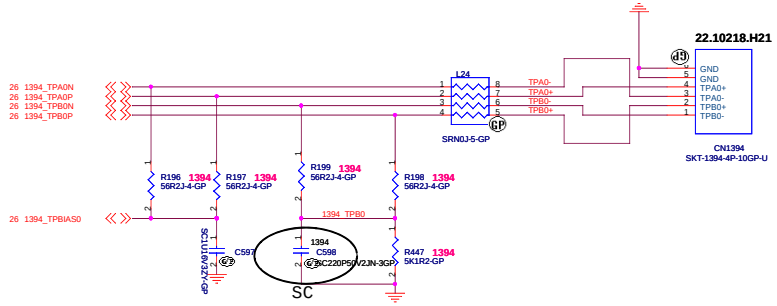


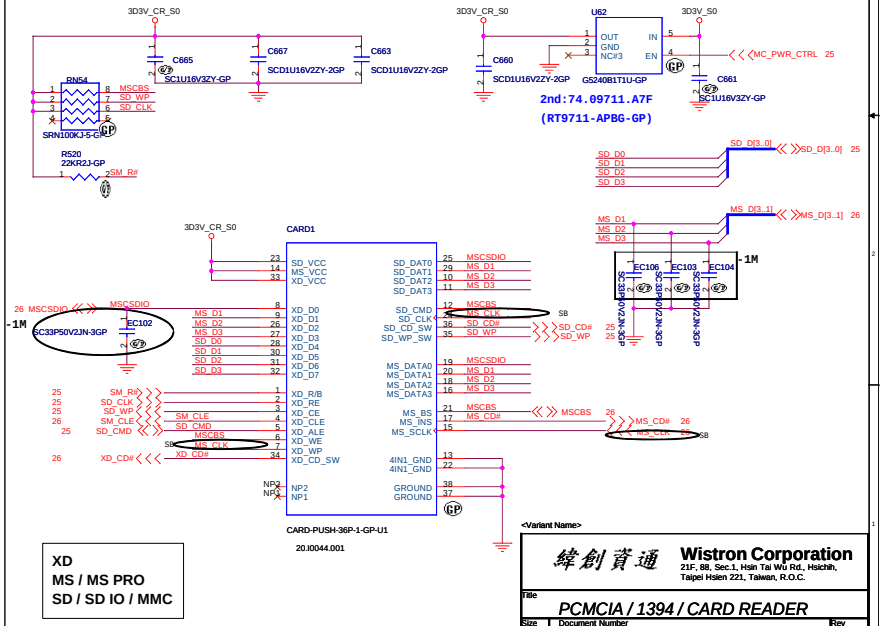
Cardbus I/F





1394 Connector





<Variant Name>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCMCIA / 1394 / CARD READER

Size	Document Number	Rev
	Columbia/Tangiz	-1M

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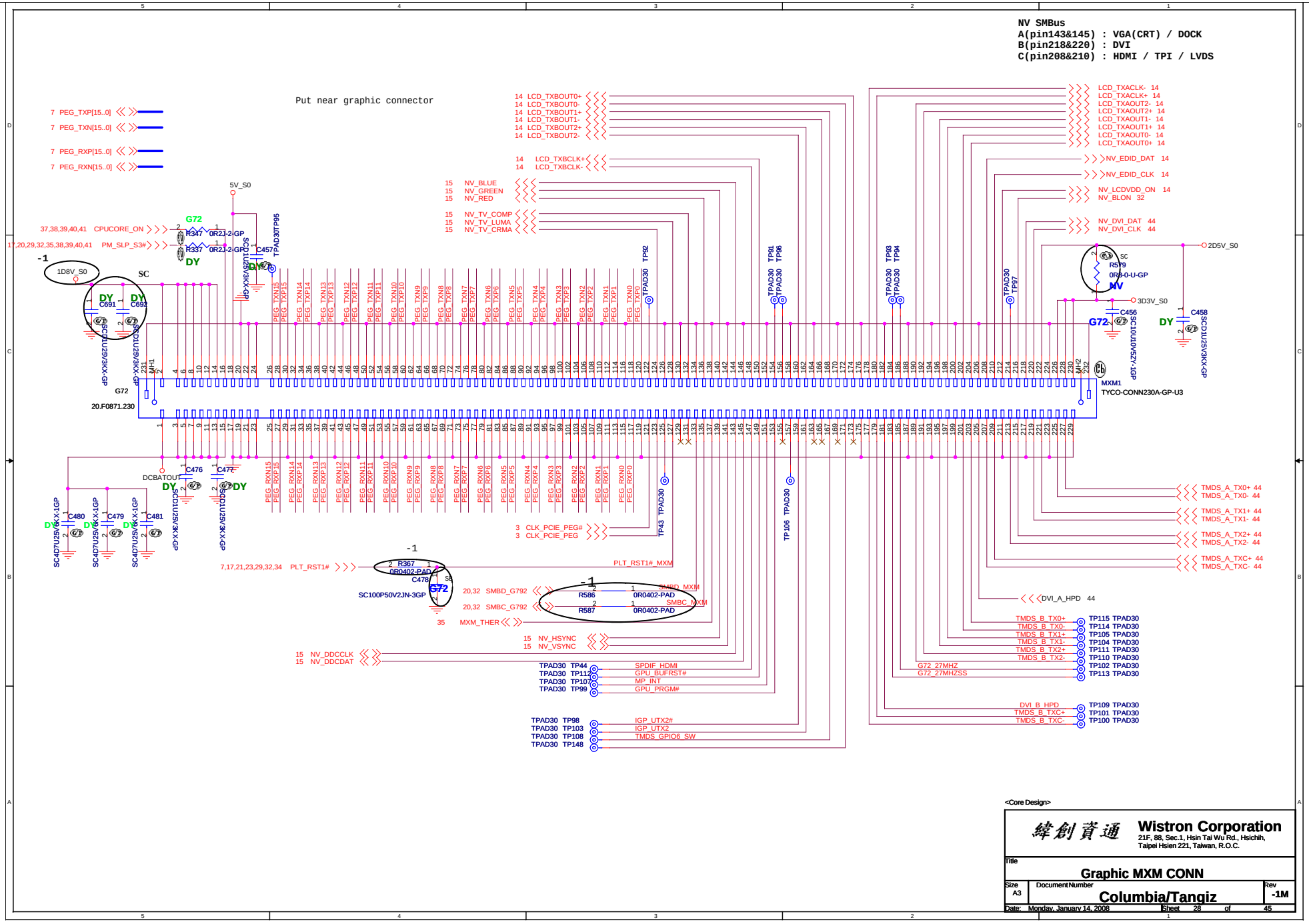

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **Graphic MXM CONN**

Size: A3 | Document Number: **Columbia/Tangiz** | Rev: -1M

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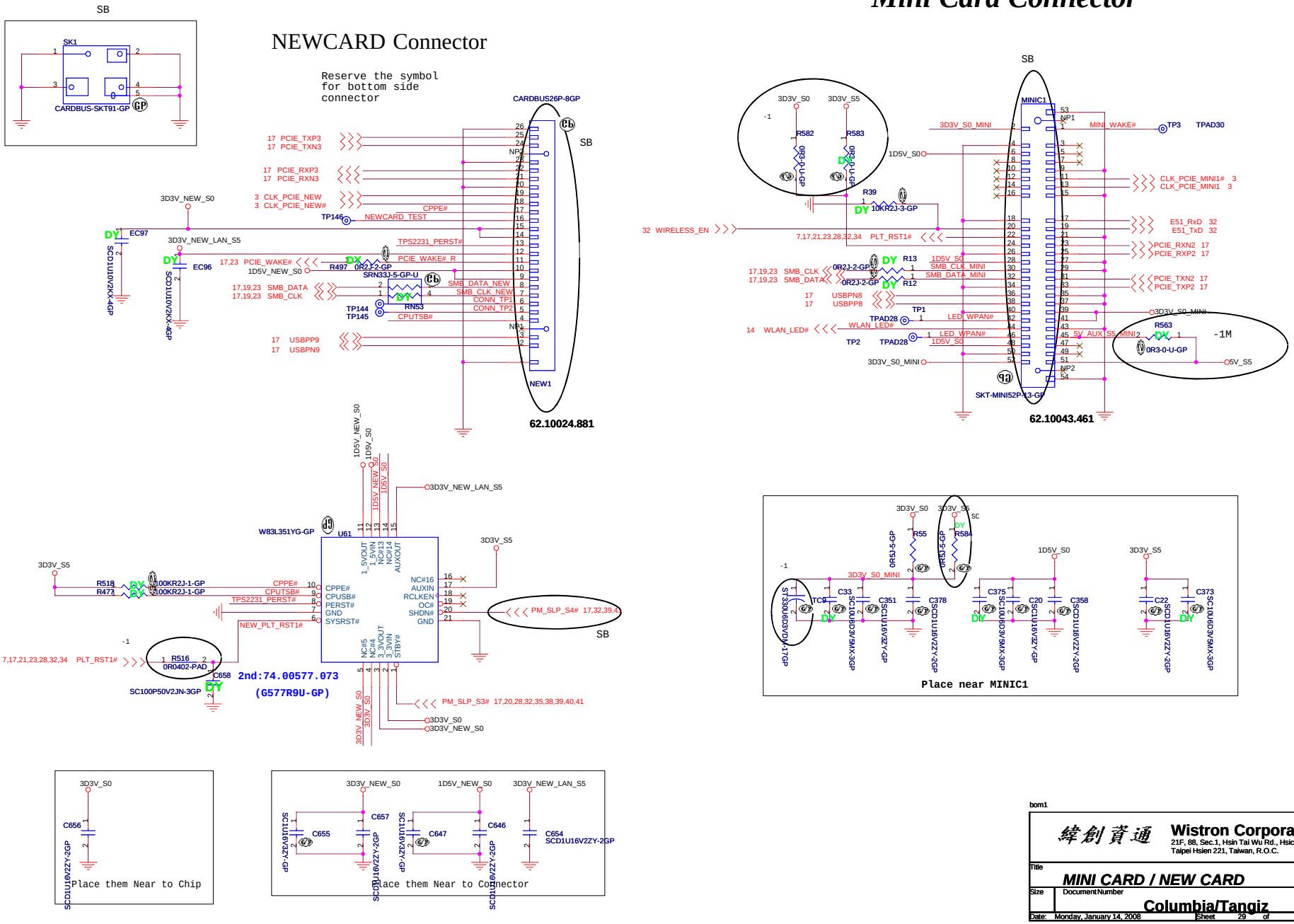
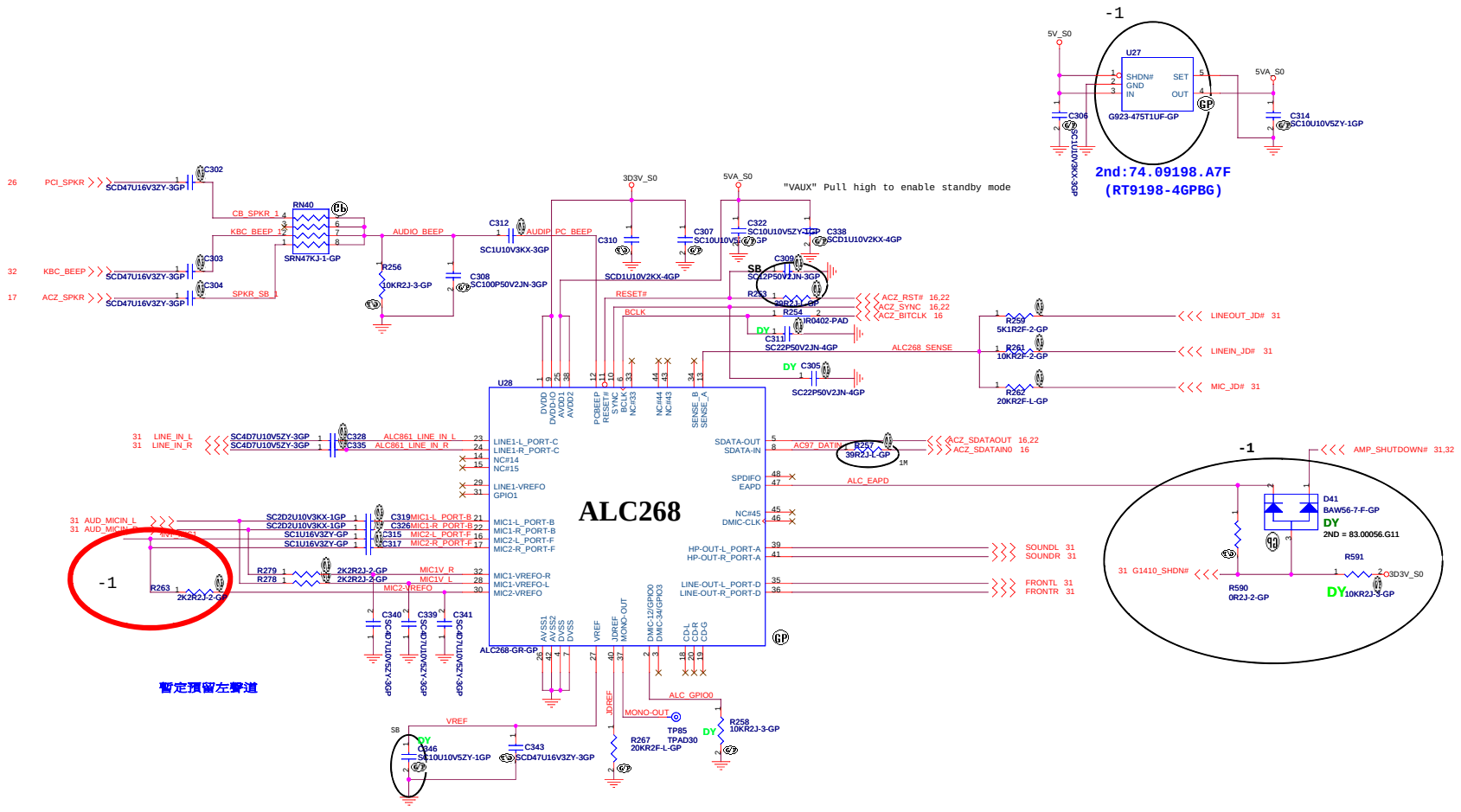
Mini Card Connector



bom1

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***MINI CARD / NEW CARD***
Size	Document Number: **Columbia/Tangiz** — Rev: -1M
Date: Monday, January 14, 2008	Sheet 29 of 45



<Variant Name>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	AZALIA CODEC - ALC268	
Size	Document Number: Columbia/Tangiz	Rev: -1M
Date: Monday, January 14, 2008	Sheet 30 of 45	

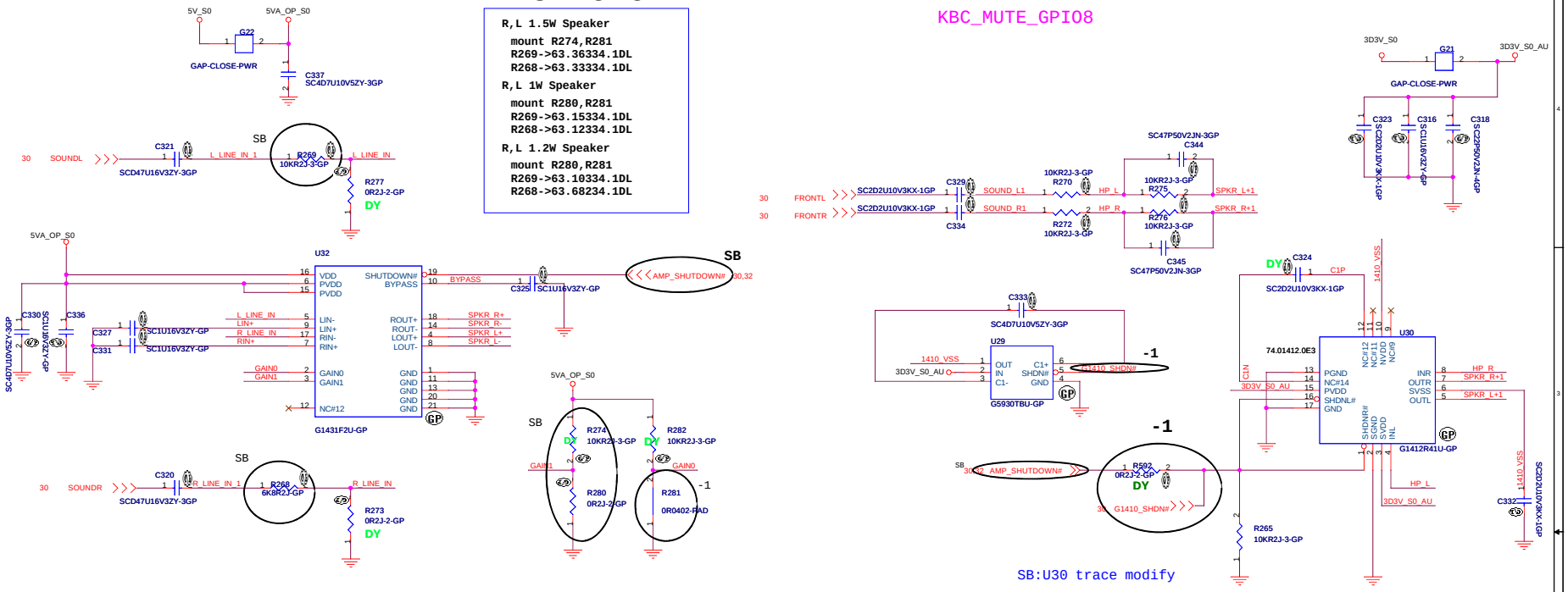
AUDIO OP AMPLIFIER

R,L 1.5W Speaker
mount R274,R281
R269->63.36334.1DL
R268->63.33334.1DL

R,L 1W Speaker
mount R280,R281
R269->63.15334.1DL
R268->63.12334.1DL

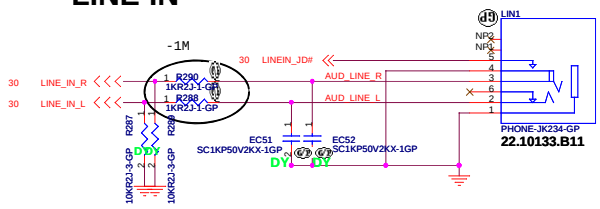
R,L 1.2W Speaker
mount R280,R281
R269->63.10334.1DL
R268->63.68234.1DL

KBC_MUTE_GPIO8

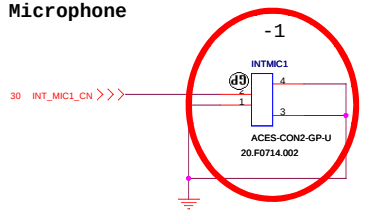


SB:U30 trace modify

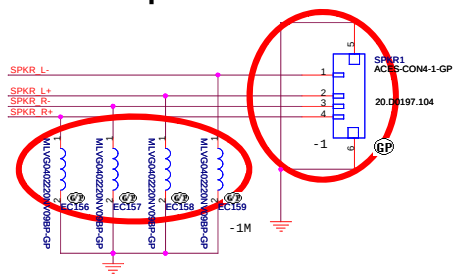
LINE IN



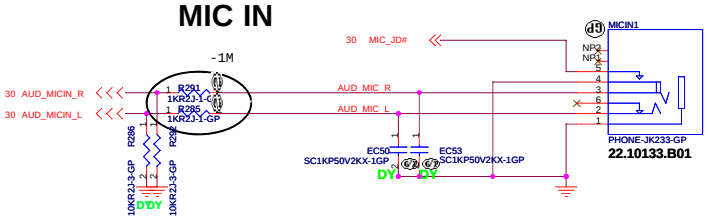
Internal Microphone



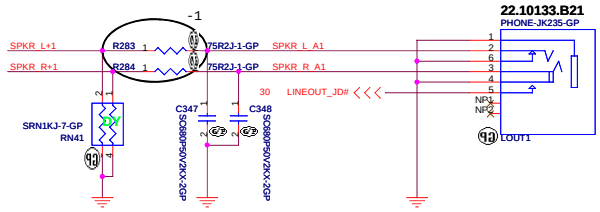
Internal Speaker



MIC IN



LINE OUT



緯創資通 Wistron Corporation
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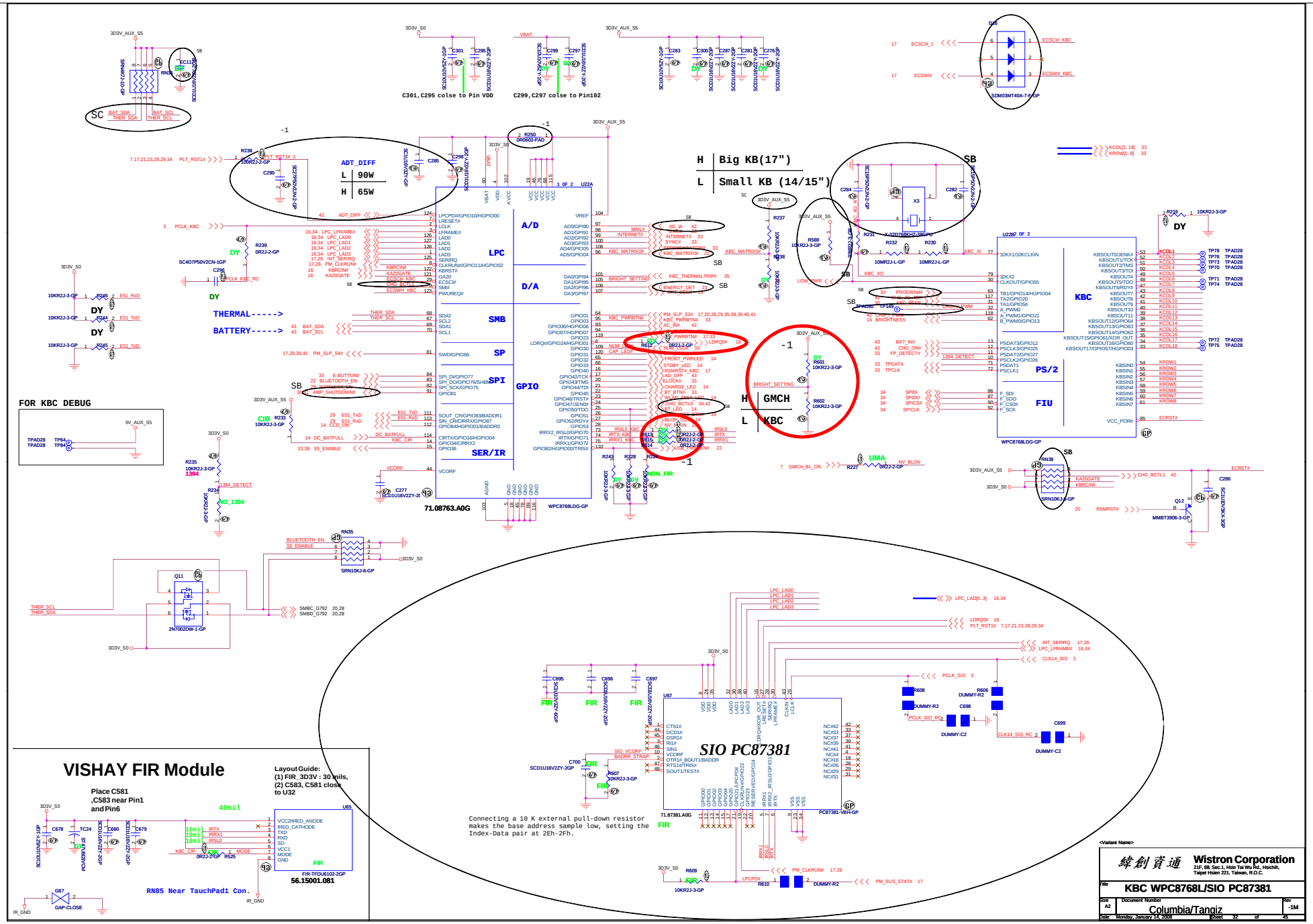
Taipei Hsien 221, Taiwan, R.O.C.

<Variant Name>

Title	AUDIO AMP AND JACK	
Size	Document Number: Columbia/Tangiz	Rev: -1
Date: Monday, January 14, 2008	Sheet 31 of 45	


ADT_DIFF
L 90W
H 65W
H Big KB(17")
L Small KB (14/15")
C301,C295 colse to Pin VDD
C299,C297 colse to Pin102
A/D
D/A
LPC
SMB
SP
SPI
GPIO
SER/IR
KBC
PS/2
FIU
WPC8768LDG-GP
71.08763.A0G
FOR KBC DEBUG
THERMAL----->
BATTERY----->
H GMCH
L KBC
NON_FIR
SIO PC87381
71.87381.A0G
PC87381-VBH-GP
Connecting a 10 K external pull-down resistor makes the base address sample low, setting the Index-Data pair at 2Eh-2Fh.
VISHAY FIR Module
Place C581 ,C583 near Pin1 and Pin6
Layout Guide:
(1) FIR_3D3V : 30 mils,
(2) C583, C581 close to U32
40mil
FIR-TFDU6102-2GP
56.15001.081
RN85 Near TauchPad1 Con.
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
KBC WPC8768L/SIO PC87381
Columbia/Tangiz
Date: Monday, January 14, 2008
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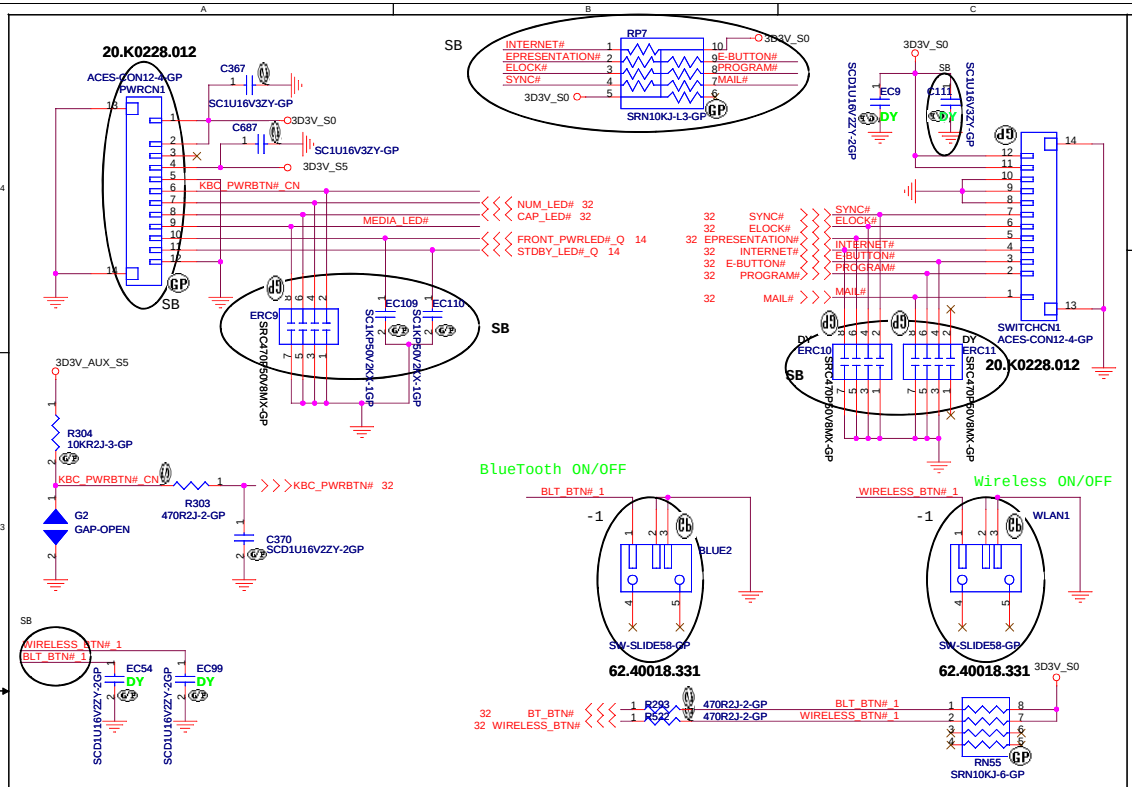
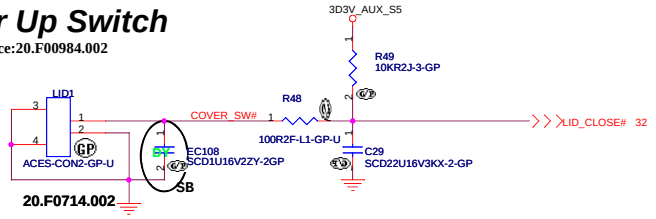
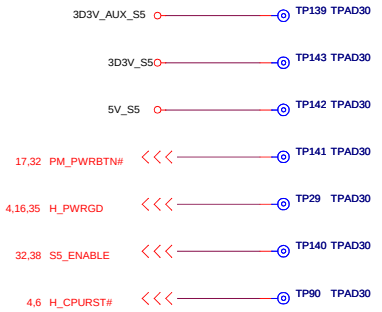


Cover Up Switch

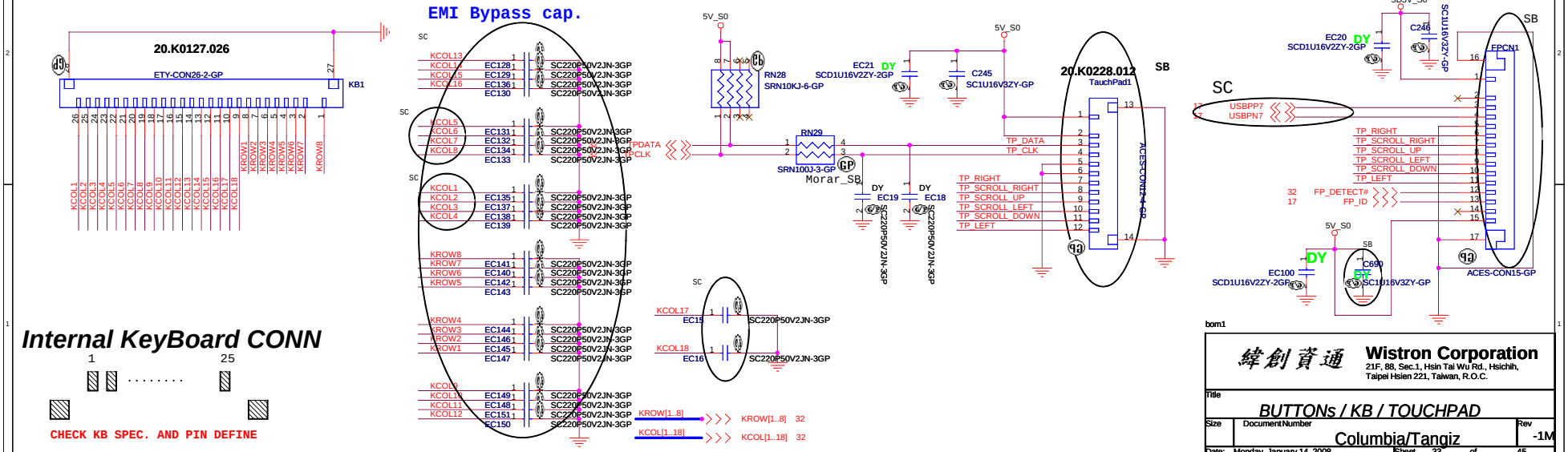
2nd source:20.F00984.002



Check test point



Test Point放在Dimm Door打開可量測處



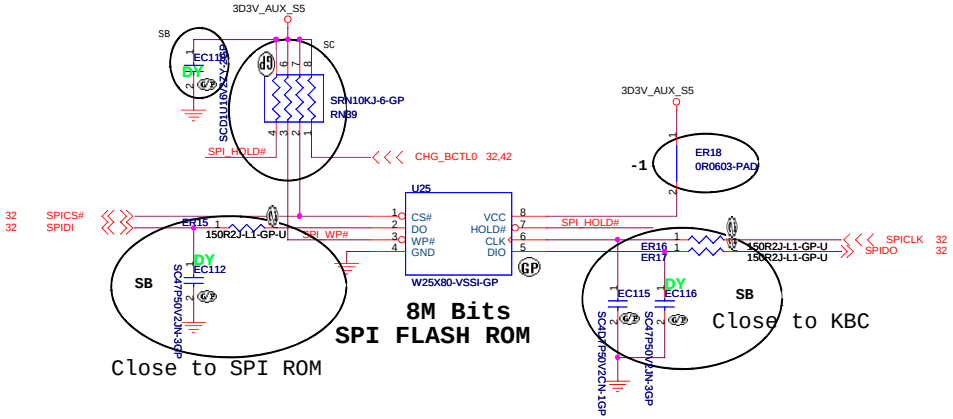
Internal KeyBoard CONN

CHECK KB SPEC. AND PIN DEFINE

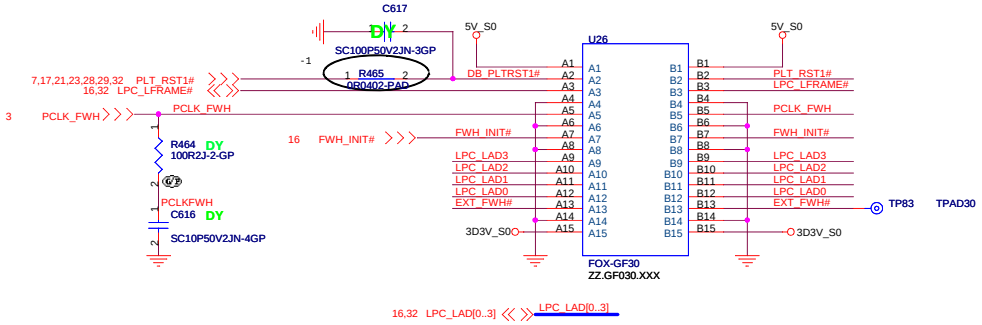
bom1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	*BUTTONs / KB / TOUCHPAD*	
Size	Document Number: Columbia/Tangiz	Rev: -1M
Date: Monday, January 14, 2008	Sheet 33 of 45	



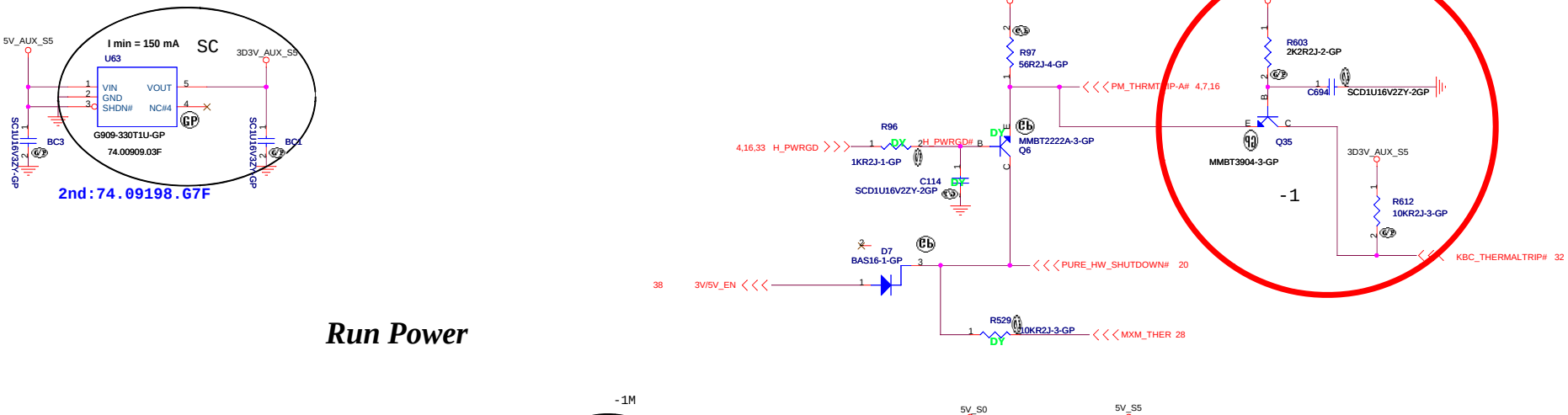
GOLDEN FINGER FOR DEBUG BOARD



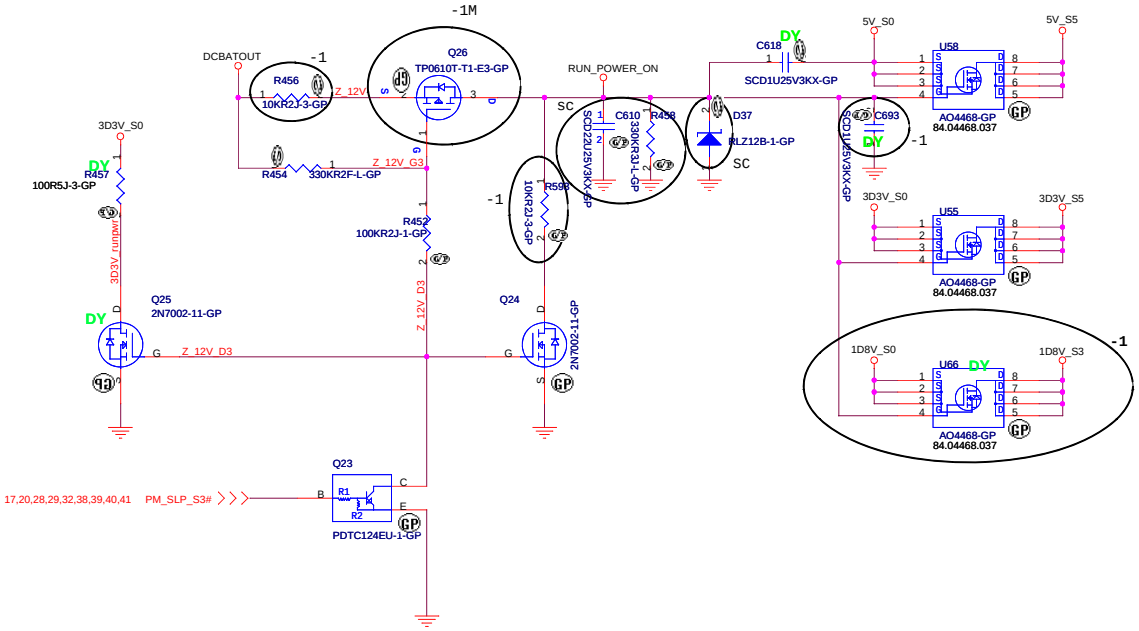
<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	BIOS	
Size A3	Document Number Columbia/Tangiz	Rev -1M
Date: Monday, January 14, 2008	Sheet 34 of 45	

Aux Power 3D3V_AUX_S5

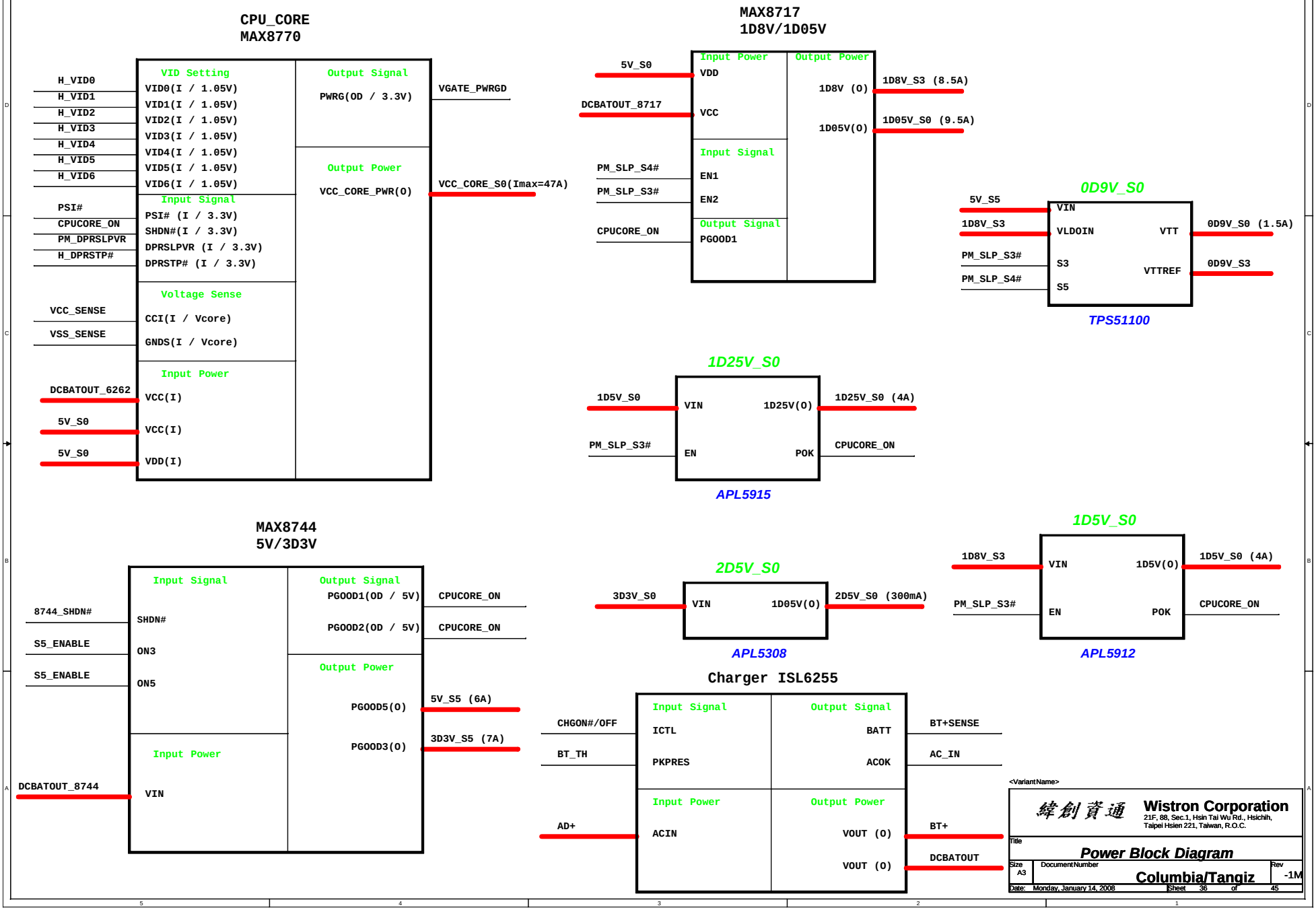


Run Power



UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***RUN POWER and 3D3V_AUX_S5***
Size / Document Number	**Columbia/Tangiz**
Rev	-1M
Date: Monday, January 14, 2008	Sheet 35 of 45


CPU_CORE
MAX8770
VID Setting
VID0(I / 1.05V)
VID1(I / 1.05V)
VID2(I / 1.05V)
VID3(I / 1.05V)
VID4(I / 1.05V)
VID5(I / 1.05V)
VID6(I / 1.05V)
Input Signal
PSI# (I / 3.3V)
SHDN#(I / 3.3V)
DPRSLPVR (I / 3.3V)
DPRSTP# (I / 3.3V)
Voltage Sense
CCI(I / Vcore)
GNDS(I / Vcore)
Input Power
VCC(I)
VCC(I)
VDD(I)
Output Signal
PWRG(OD / 3.3V)
Output Power
VCC_CORE_PWR(O)
H_VID0
H_VID1
H_VID2
H_VID3
H_VID4
H_VID5
H_VID6
PSI#
CPUCORE_ON
PM_DPRSLPVR
H_DPRSTP#
VCC_SENSE
VSS_SENSE
DCBATOUT_6262
5V_S0
5V_S0
VGATE_PWRGD
VCC_CORE_S0(Imax=47A)
MAX8717
1D8V/1D05V
Input Power
VDD
VCC
Input Signal
EN1
EN2
Output Signal
PGOOD1
Output Power
1D8V (O)
1D05V(O)
5V_S0
DCBATOUT_8717
PM_SLP_S4#
PM_SLP_S3#
CPUCORE_ON
1D8V_S3 (8.5A)
1D05V_S0 (9.5A)
0D9V_S0
VIN
VLDOIN
S3
S5
VTT
VTTREF
5V_S5
1D8V_S3
PM_SLP_S3#
PM_SLP_S4#
0D9V_S0 (1.5A)
0D9V_S3
TPS51100
1D25V_S0
VIN
EN
1D25V(O)
POK
1D5V_S0
PM_SLP_S3#
1D25V_S0 (4A)
CPUCORE_ON
APL5915
MAX8744
5V/3D3V
Input Signal
SHDN#
ON3
ON5
Input Power
VIN
Output Signal
PGOOD1(OD / 5V)
PGOOD2(OD / 5V)
Output Power
PGOOD5(O)
PGOOD3(O)
8744_SHDN#
S5_ENABLE
S5_ENABLE
DCBATOUT_8744
CPUCORE_ON
CPUCORE_ON
5V_S5 (6A)
3D3V_S5 (7A)
2D5V_S0
VIN
1D05V(O)
3D3V_S0
2D5V_S0 (300mA)
APL5308
1D5V_S0
VIN
EN
1D5V(O)
POK
1D8V_S3
PM_SLP_S3#
1D5V_S0 (4A)
CPUCORE_ON
APL5912
Charger ISL6255
Input Signal
ICTL
PKPRES
Input Power
ACIN
Output Signal
BATT
ACOK
Output Power
VOUT (O)
VOUT (O)
CHGON#/OFF
BT_TH
AD+
BT+SENSE
AC_IN
BT+
DCBATOUT
<VariantName>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Power Block Diagram
Size
A3
Document Number
Columbia/Tangiz
Rev
-1M
Date: Monday, January 14, 2008
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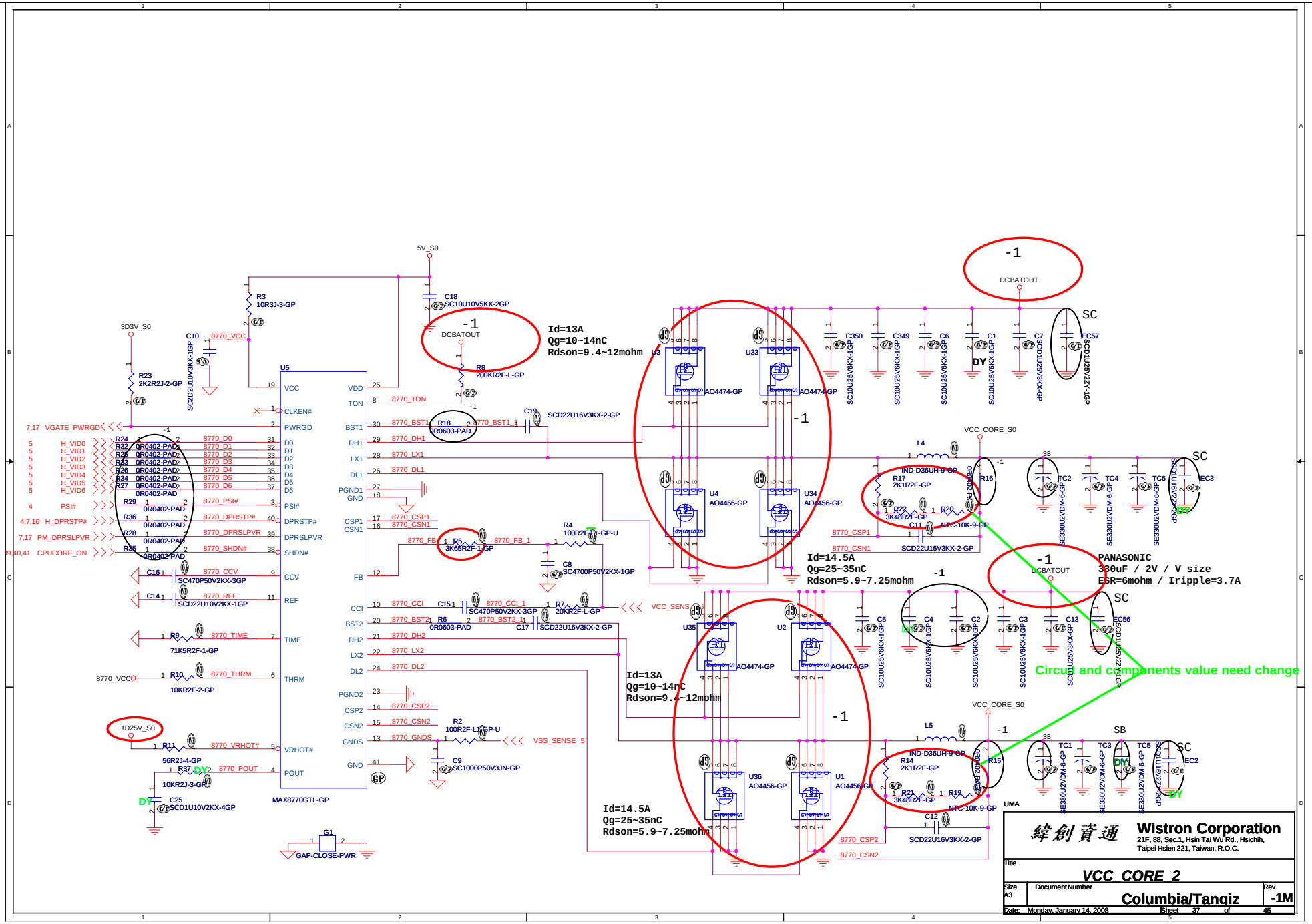
5V_S0
3D3V_S0
1D25V_S0
DCBATOUT
VCC_CORE_S0
U5
MAX8770GTL-GP
VCC
CLKEN#
PWRGD
D0
D1
D2
D3
D4
D5
D6
PSI#
DPRSTP#
DPRSLPVR
SHDN#
CCV
REF
TIME
THRM
VRHOT#
POUT
VDD
TON
BST1
DH1
LX1
DL1
PGND1
GND
CSP1
CSN1
FB
CCI
BST2
DH2
LX2
DL2
PGND2
CSP2
CSN2
GNDS
Id=13A
Qg=10~14nC
Rdson=9.4~12mohm
Id=14.5A
Qg=25~35nC
Rdson=5.9~7.25mohm
Id=13A
Qg=10~14nC
Rdson=9.4~12mohm
Id=14.5A
Qg=25~35nC
Rdson=5.9~7.25mohm
PANASONIC
330uF / 2V / V size
ESR=6mohm / Iripple=3.7A
Circuit and components value need change
VCC_SENS
VSS_SENSE
GAP-CLOSE-PWR
UMA
SB
SC
DY
-1
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
VCC_CORE_2
Size
A3
Document Number
Columbia/Tangiz
Rev
-1M
Date: Monday, January 14, 2008
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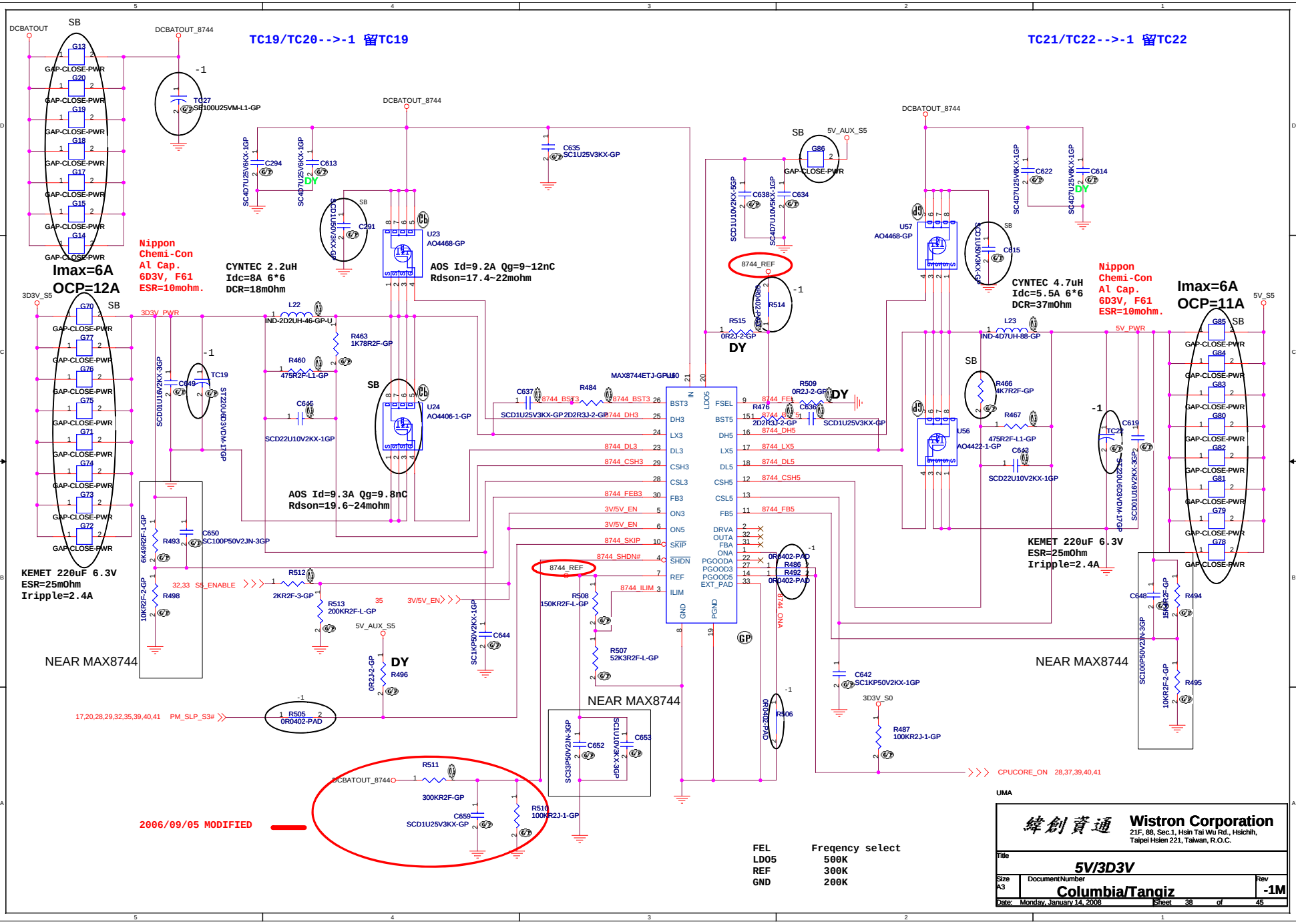
TC19/TC20-->-1 留TC19
TC21/TC22-->-1 留TC22
Imax=6A
OCP=12A
Nippon Chemi-Con Al Cap. 6D3V, F61 ESR=10mohm.
CYNTEC 2.2uH Idc=8A 6*6 DCR=18mOhm
AOS Id=9.2A Qg=9~12nC Rdson=17.4~22mohm
AOS Id=9.3A Qg=9.8nC Rdson=19.6~24mohm
KEMET 220uF 6.3V ESR=25mOhm Iripple=2.4A
NEAR MAX8744
MAX8744ETJ-GPU60
CYNTEC 4.7uH Idc=5.5A 6*6 DCR=37mOhm
Imax=6A
OCP=11A
KEMET 220uF 6.3V ESR=25mOhm Iripple=2.4A
2006/09/05 MODIFIED
FEL Freqency select
LDO5 500K
REF 300K
GND 200K
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title 5V/3D3V
Size A3
Document Number Columbia/Tangiz
Rev -1M
Date: Monday, January 14, 2008
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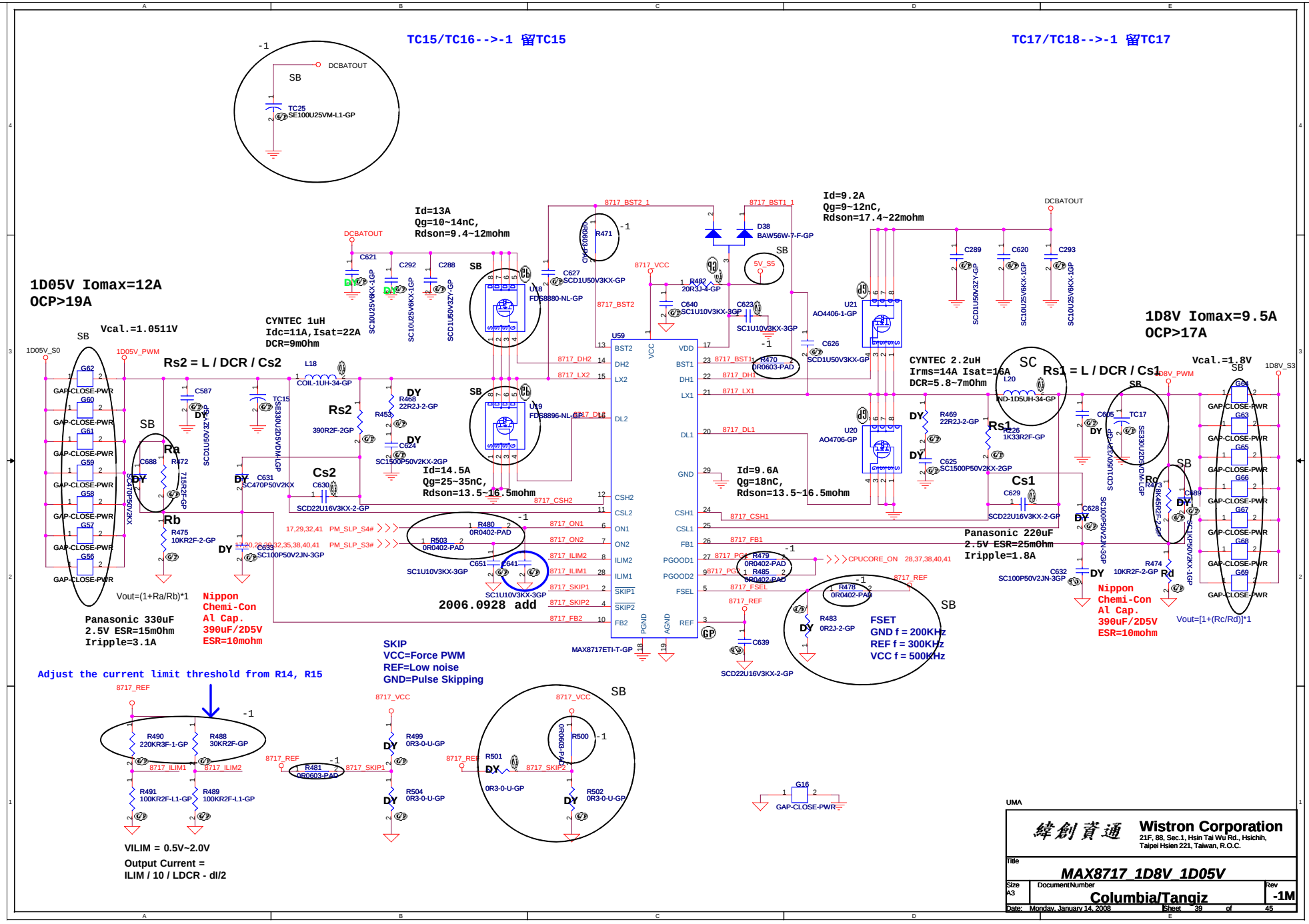

UMA

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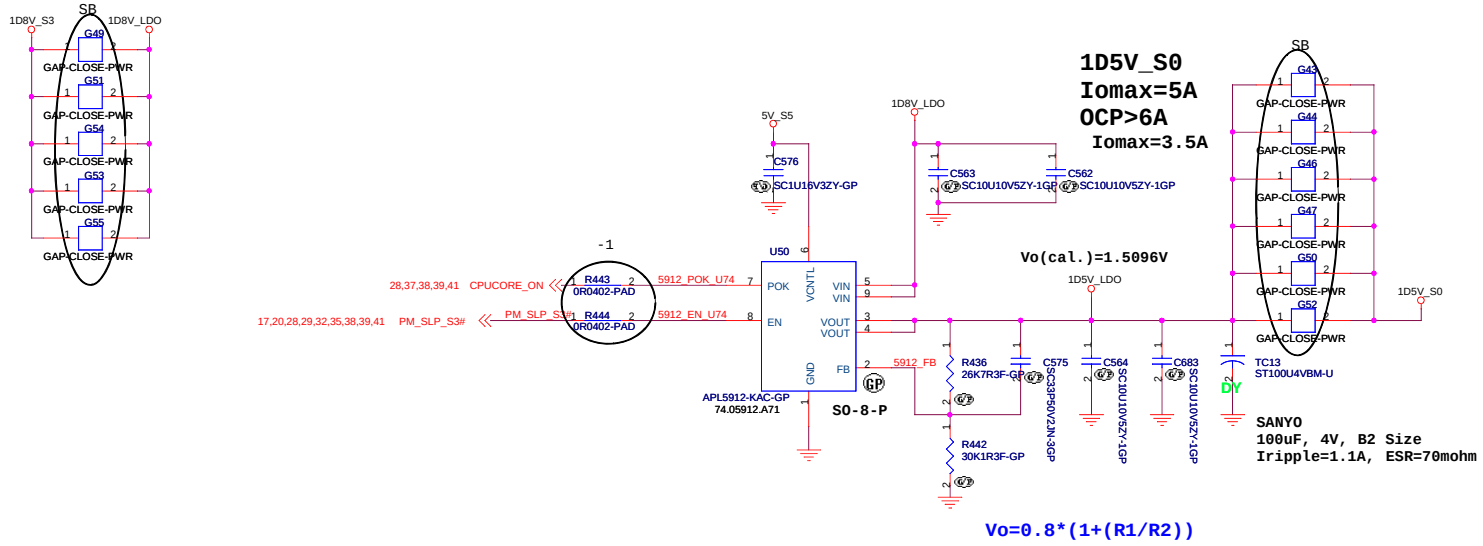
Taipei Hsien 221, Taiwan, R.O.C.

Title: **MAX8717_1D8V_1D05V**

Size: A3 | Document Number: **Columbia/Tangiz** | Rev: **-1M**

Date: Monday, January 14, 2008 | Sheet 39 of 45



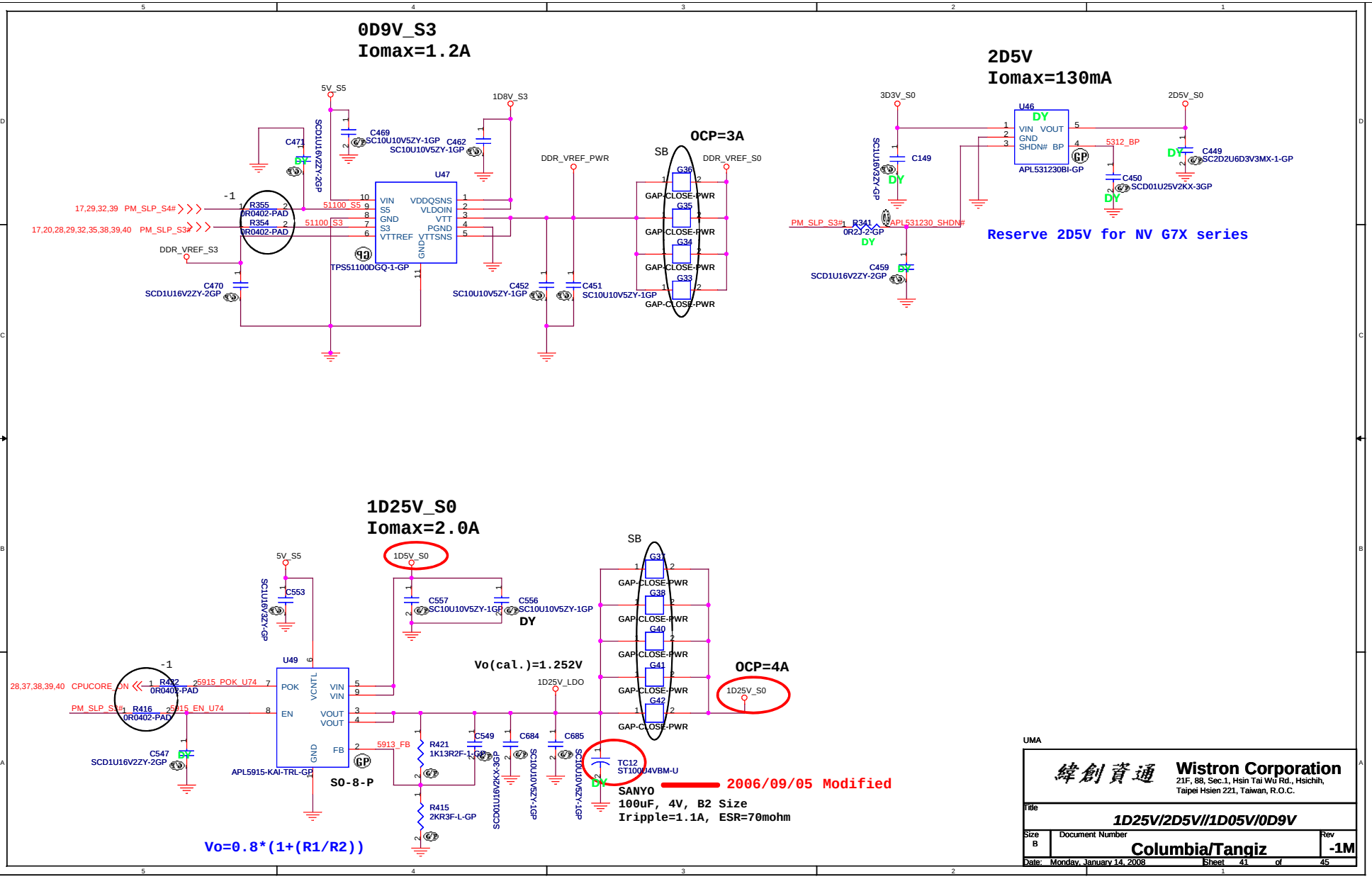
UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***APW5912_1D5V***

Size | Document Number: **Columbia/Tangiz** | Rev: -1M

Date: Monday, January 14, 2008 | Sheet 40 of 45


0D9V_S3
Iomax=1.2A
5V_S5
1D8V_S3
C469
SC10U10V5ZY-1GP
C462
SC10U10V5ZY-1GP
C471
SCD1U16V2ZY-2GP
U47
VIN
S5
GND
S3
VTTREF
VDDQSNS
VLDOIN
VTT
PGND
VTTSNS
GND
TPS51100DGQ-1-GP
17,29,32,39 PM_SLP_S4#
17,20,28,29,32,35,38,39,40 PM_SLP_S3#
R355
0R0402-PAD
R354
0R0402-PAD
51100_S5
51100_S3
DDR_VREF_S3
C470
SCD1U16V2ZY-2GP
DDR_VREF_PWR
C452
SC10U10V5ZY-1GP
C451
SC10U10V5ZY-1GP
SB
OCP=3A
DDR_VREF_S0
G36
G35
G34
G33
GAP-CLOSE-PWR
2D5V
Iomax=130mA
3D3V_S0
2D5V_S0
U46
VIN
VOUT
GND
SHDN#
BP
APL531230BI-GP
5312_BP
C149
SCD1U16V2ZY-2GP
C449
SC2D2U6D3V3MX-1-GP
C450
SCD01U25V2KX-3GP
PM_SLP_S3#
R341
0R2J-2-GP
APL531230_SHDN#
C459
SCD1U16V2ZY-2GP
Reserve 2D5V for NV G7X series
1D25V_S0
Iomax=2.0A
5V_S5
1D5V_S0
C553
SC1U16V3ZY-GP
C557
SC10U10V5ZY-1GP
C556
SC10U10V5ZY-1GP
DY
U49
POK
EN
VCNTL
VIN
VOUT
GND
FB
APL5915-KAI-TRL-GP
SO-8-P
28,37,38,39,40 CPUCORE_ON
R432
0R0402-PAD
5915_POK_U74
PM_SLP_S4#
R416
0R0402-PAD
5915_EN_U74
C547
SCD1U16V2ZY-2GP
5913_FB
Vo(cal.)=1.252V
1D25V_LDO
R421
1K13R2F-1-GP
C549
SCD1U16V2KX-3GP
C684
SC10U10V5ZY-1GP
C685
SC10U10V5ZY-1GP
R415
2KR3F-L-GP
Vo=0.8*(1+(R1/R2))
SB
G37
G38
G40
G41
G42
GAP-CLOSE-PWR
OCP=4A
1D25V_S0
TC12
ST100U4VBM-U
SANYO
100uF, 4V, B2 Size
Iripple=1.1A, ESR=70mohm
2006/09/05 Modified
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
1D25V/2D5V//1D05V/0D9V
Size
B
Document Number
Columbia/Tangiz
Rev
-1M
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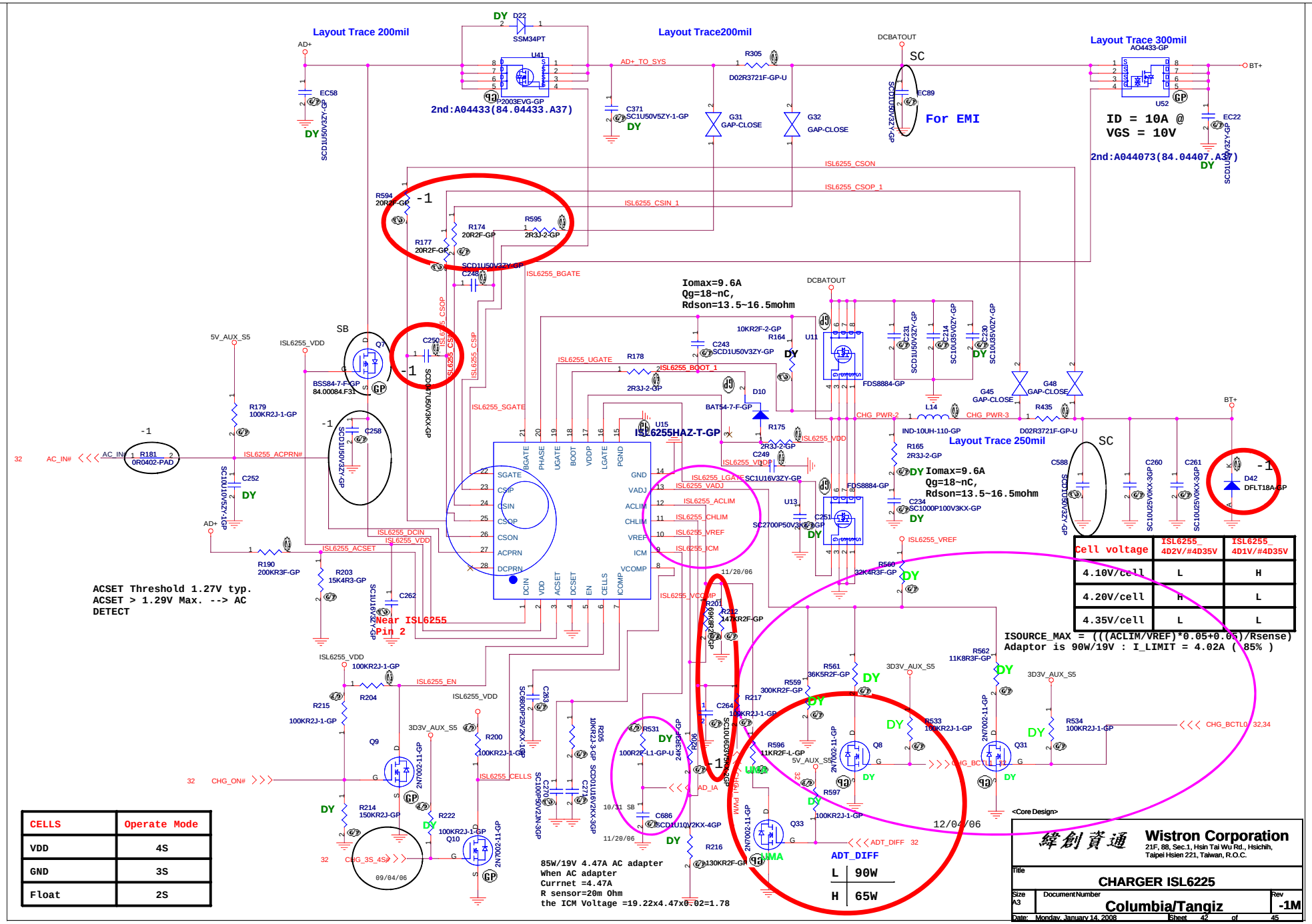
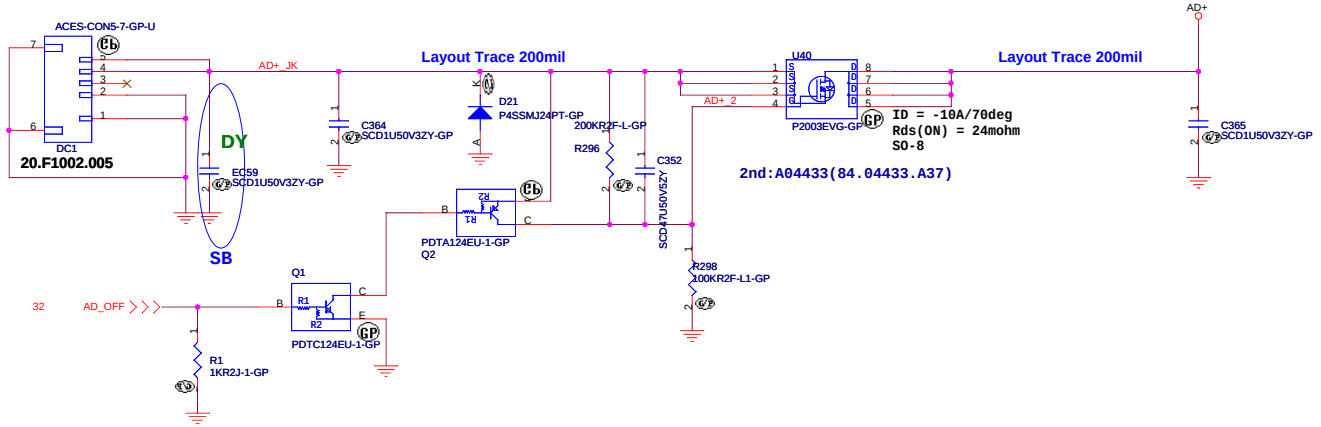


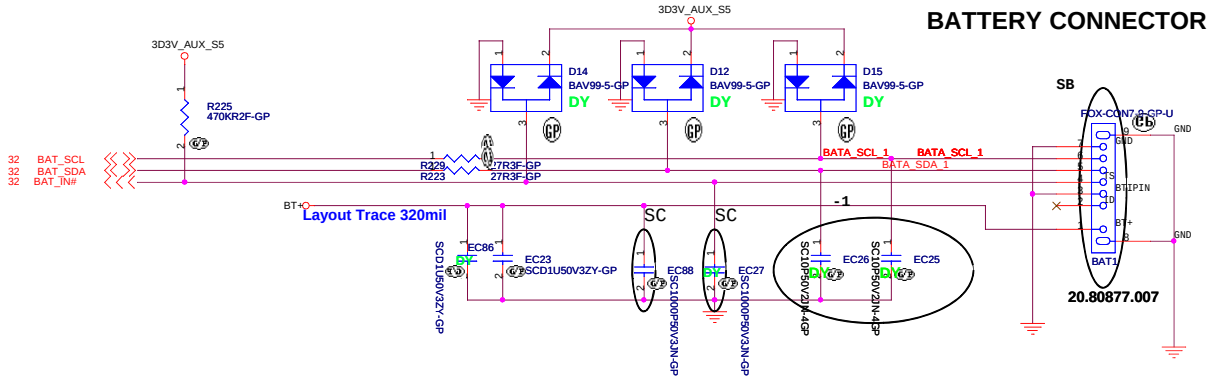
Cell voltage	ISL6255_ 4D2V/#4D35V	ISL6255_ 4D1V/#4D35V
4.10V/cell	L	H
4.20V/cell	H	L
4.35V/cell	L	L

CELLS	Operate Mode
VDD	4S
GND	3S
Float	2S

Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



<Variant Name>

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Title	**AD/BATT CONN**
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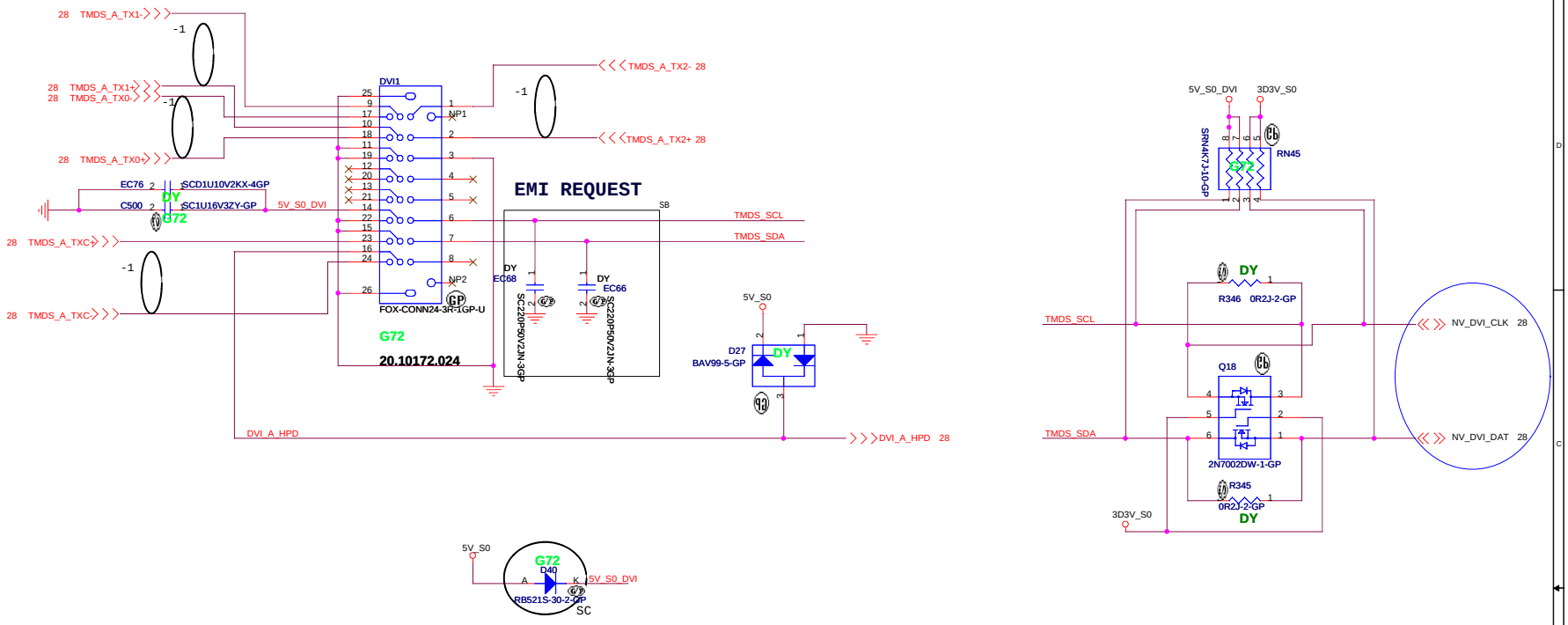

<Variant Name>

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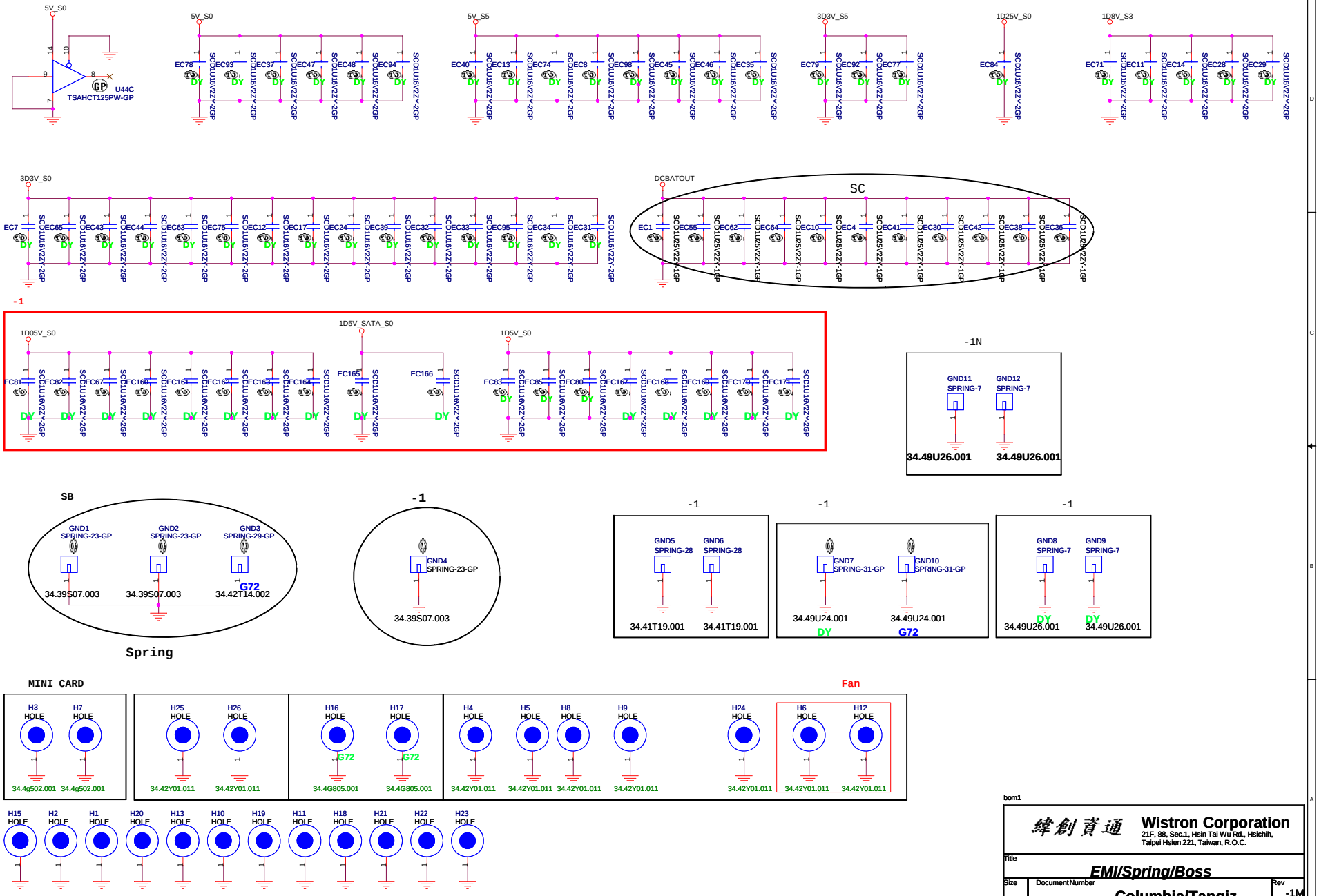
Title	**DVI CONNECTOR**
Size A3	Document Number **Columbia/Tangiz** Rev **-1M**
Date: Monday, January 14, 2008	Sheet 44 of 45



bom1

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